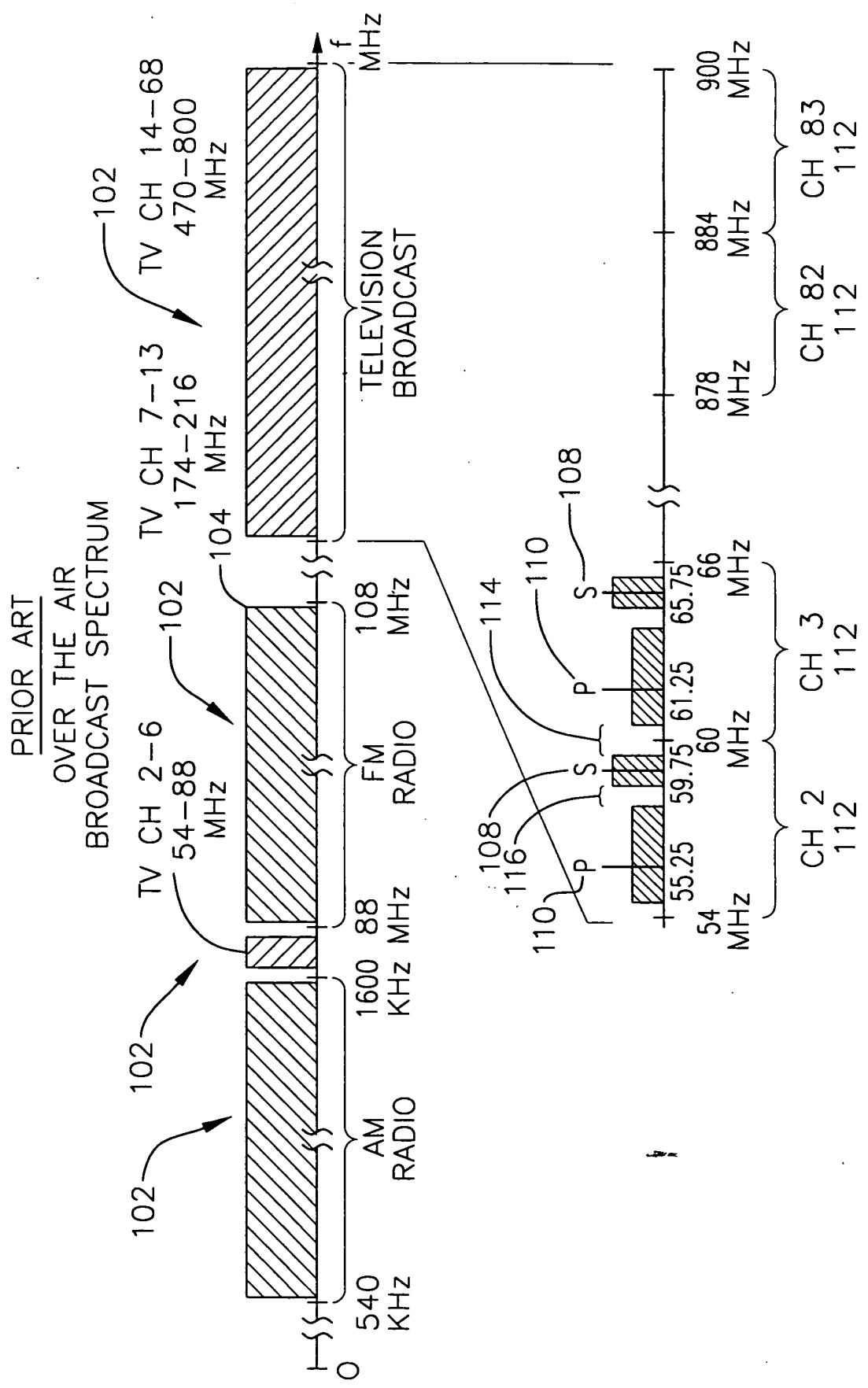


FIG. 1



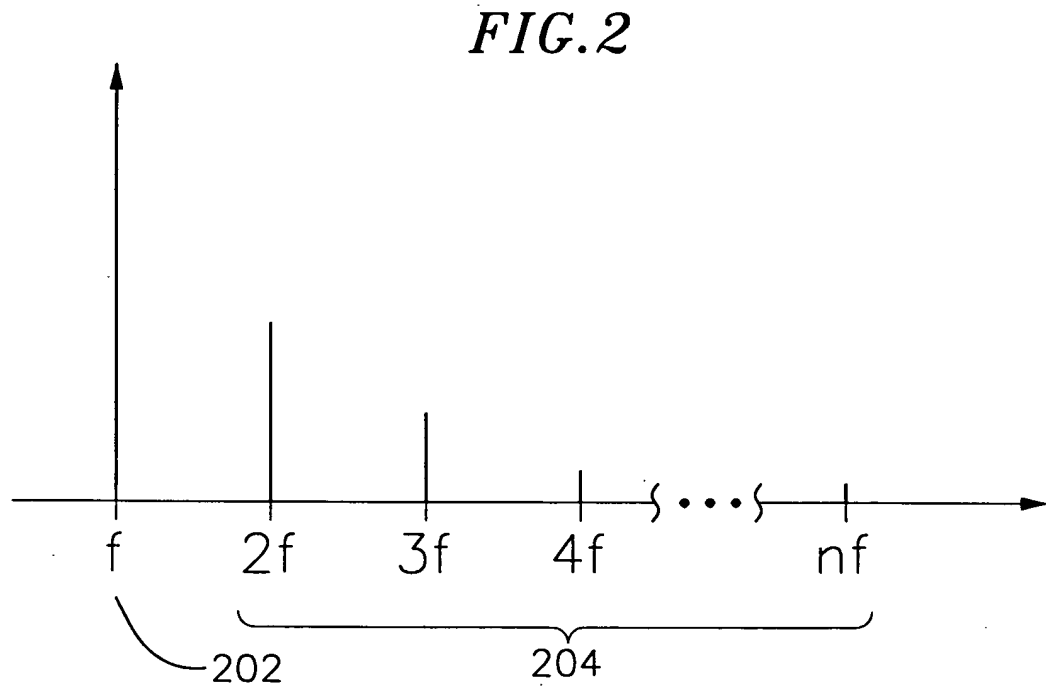


FIG. 3
PRIOR ART

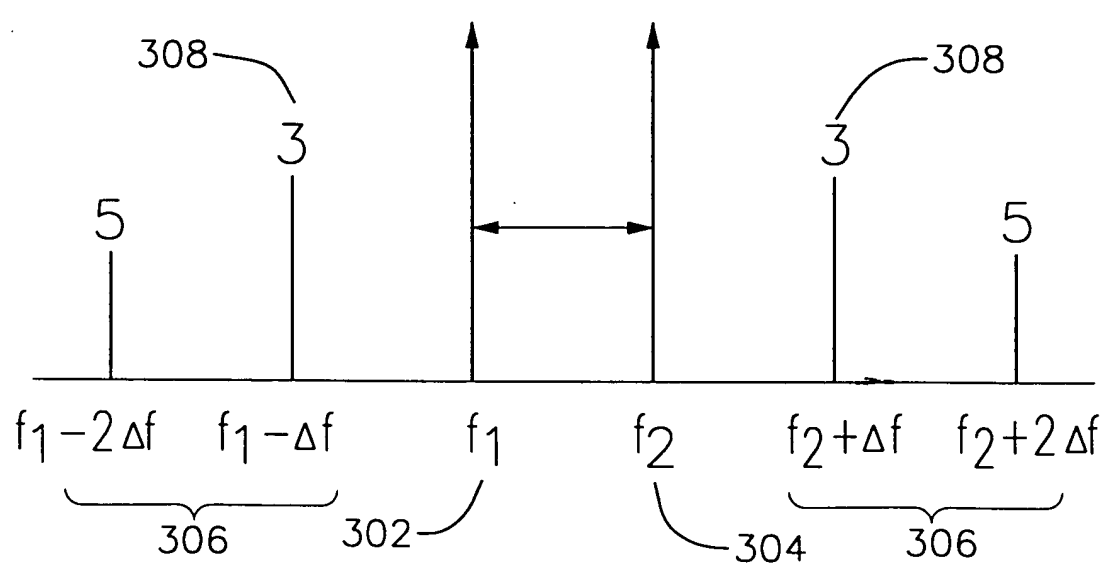


FIG. 4
PRIOR ART

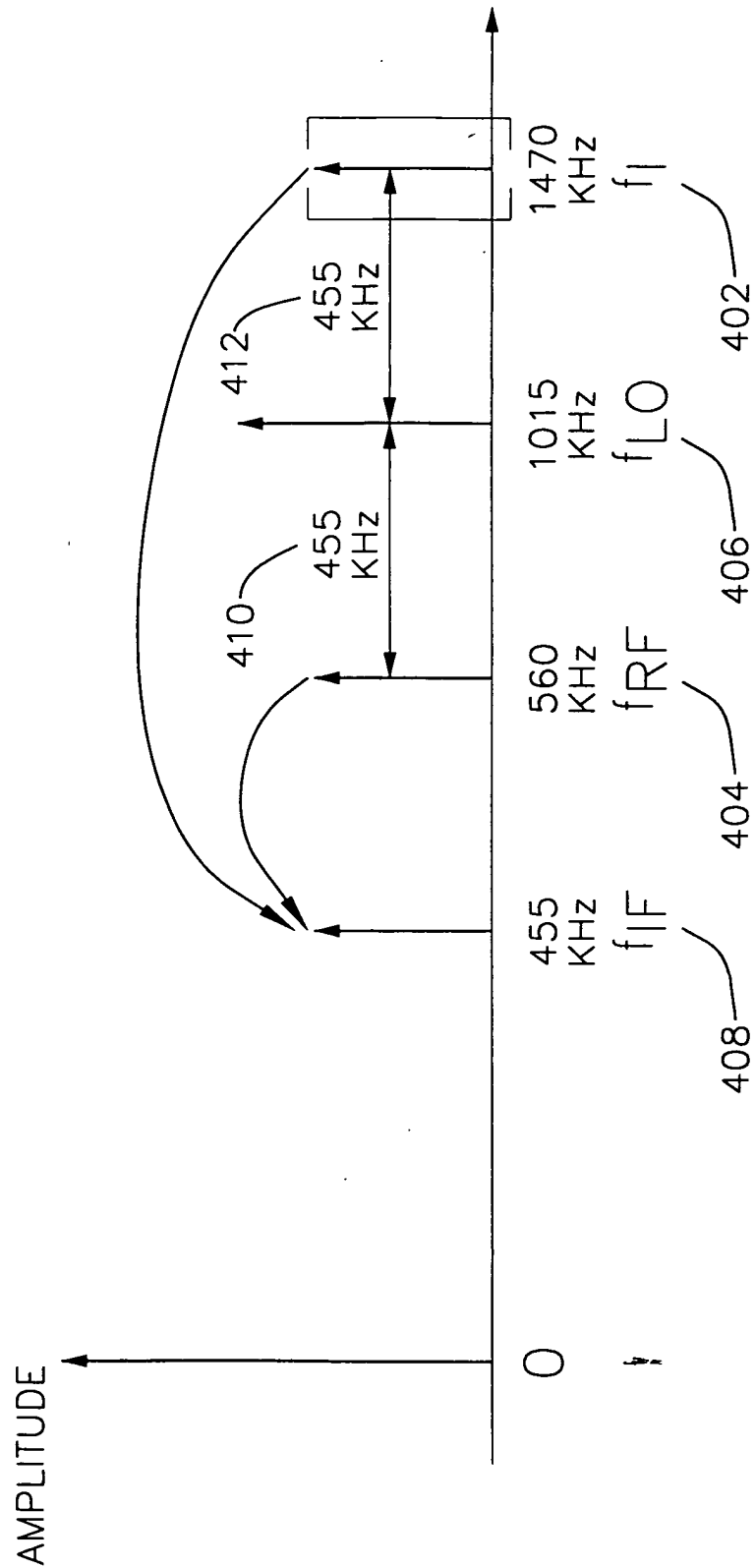
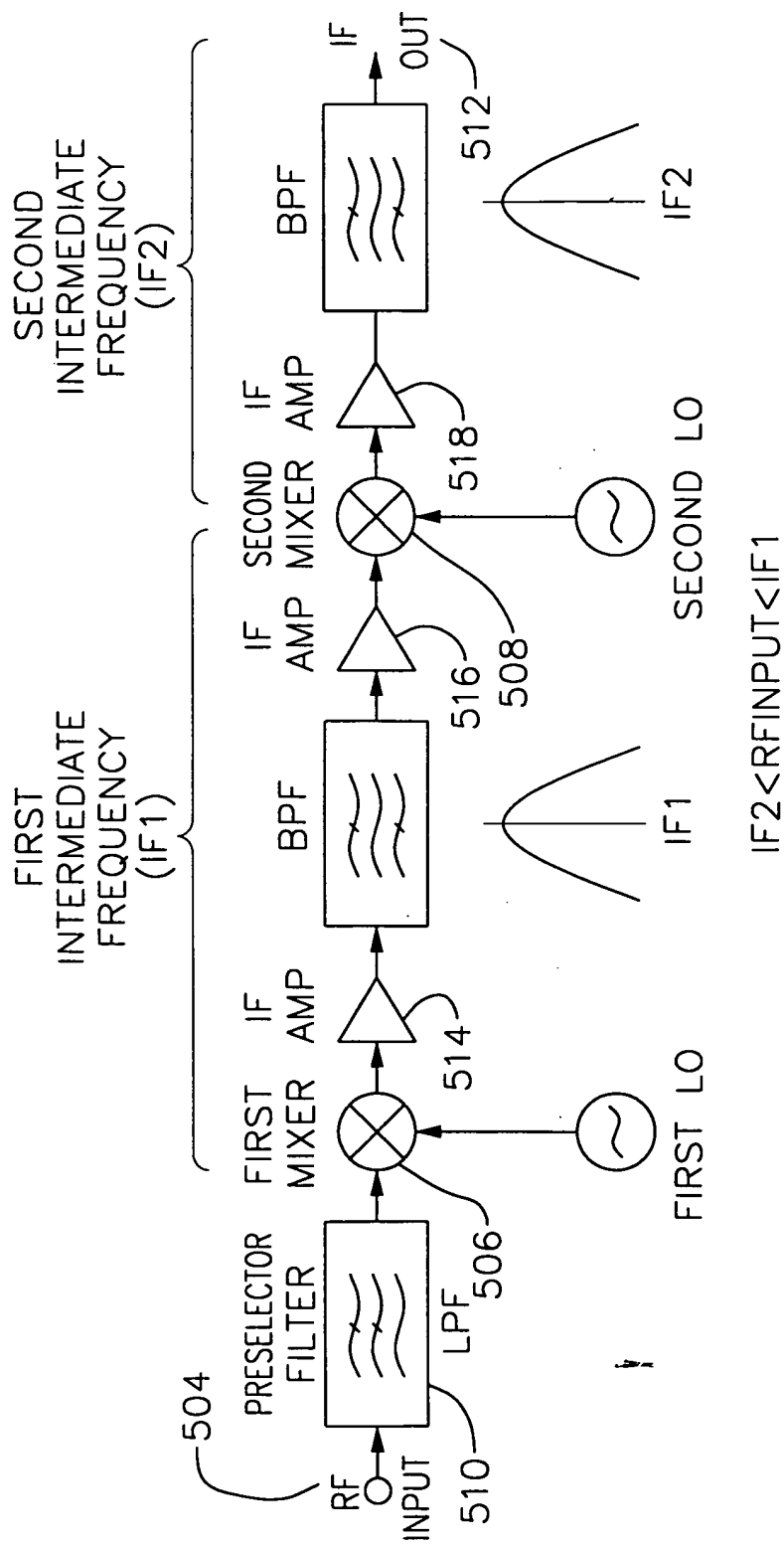


FIG. 5

DUAL CONVERSION RECEIVER



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FIG. 6

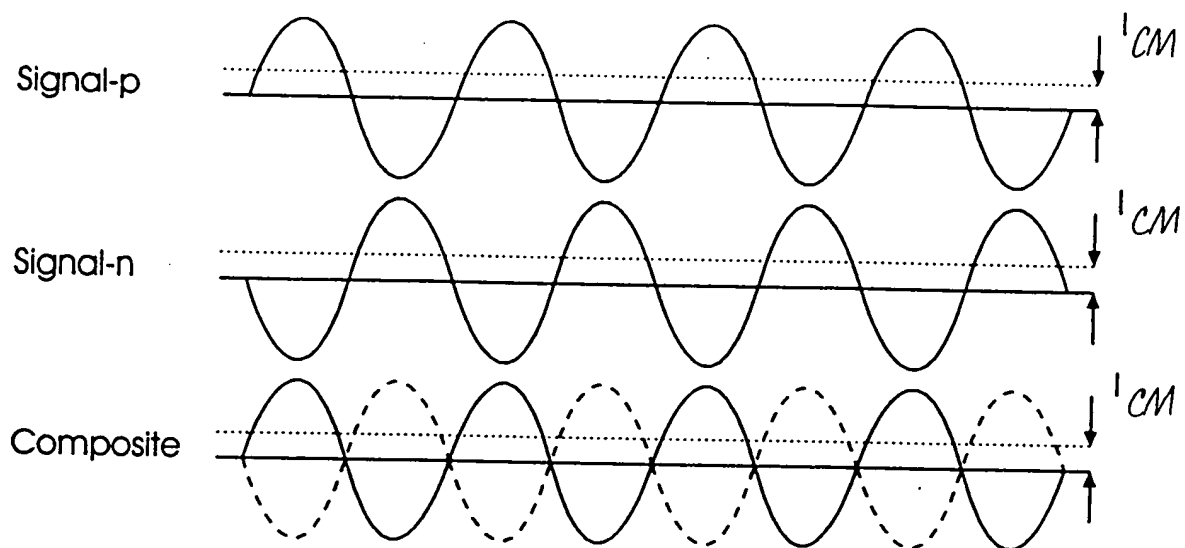
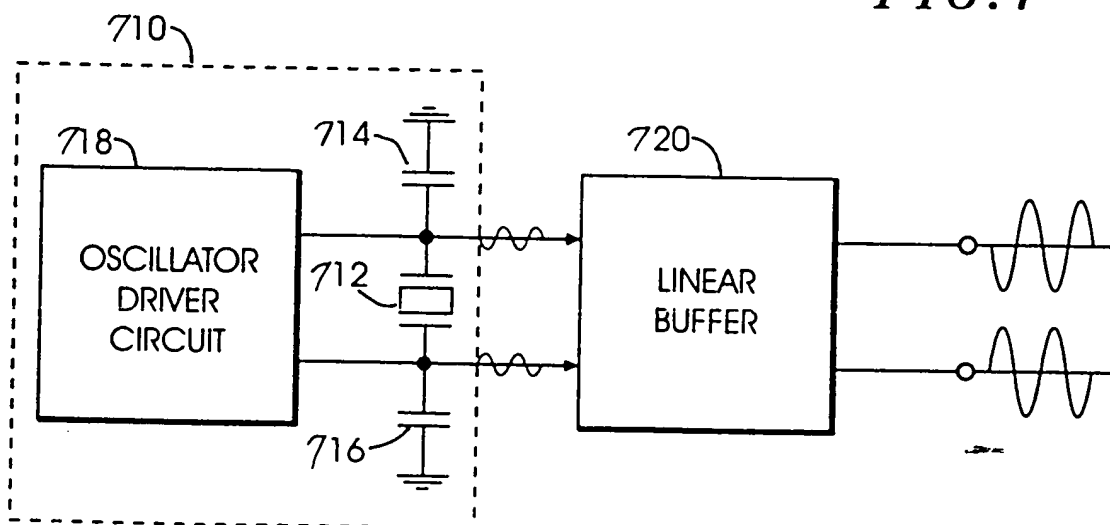


FIG. 7



0966072 01001

FIG. 8

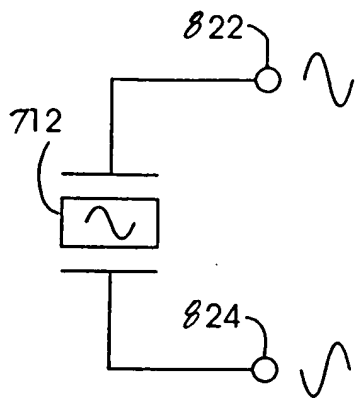


FIG. 9

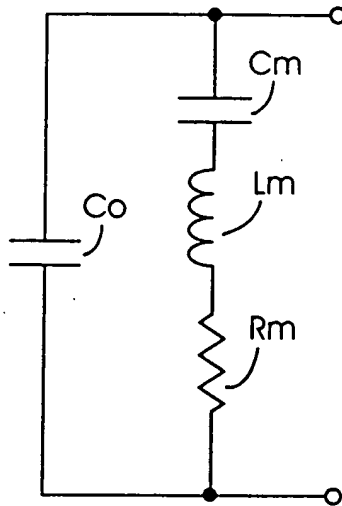


FIG. 10

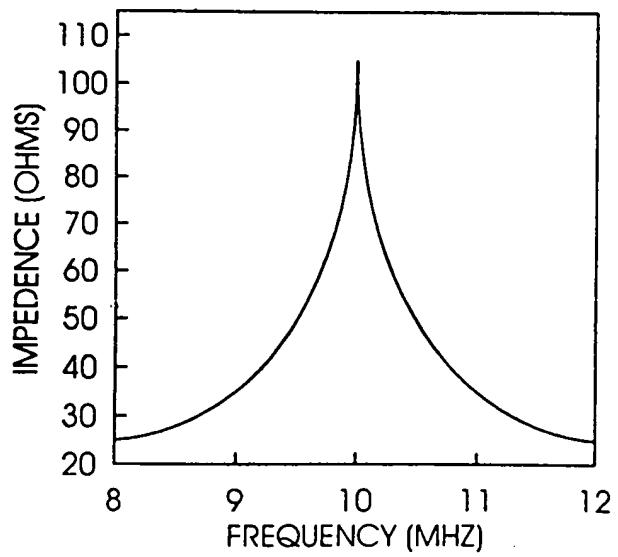
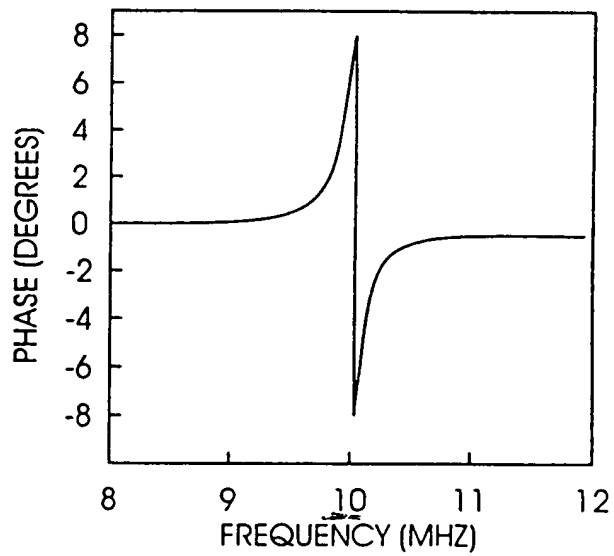


FIG. 11



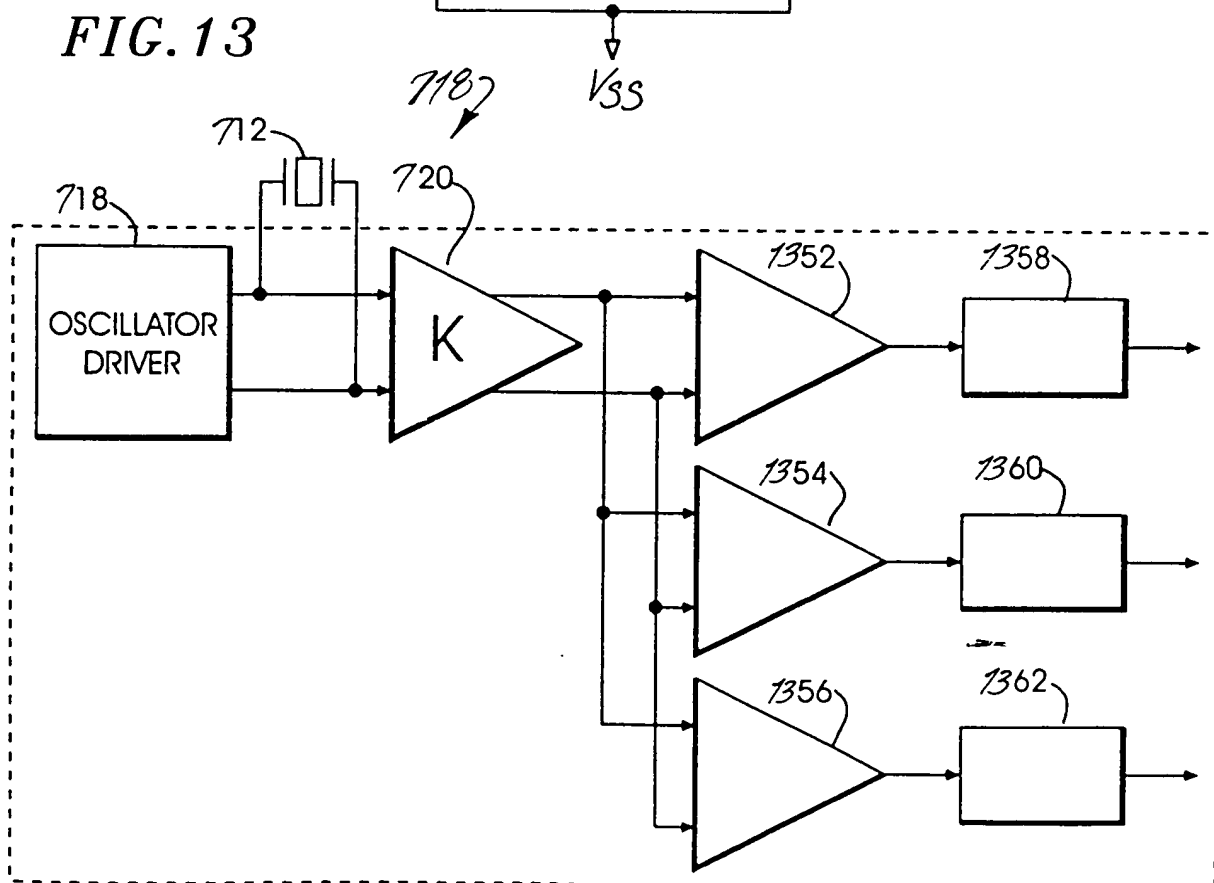
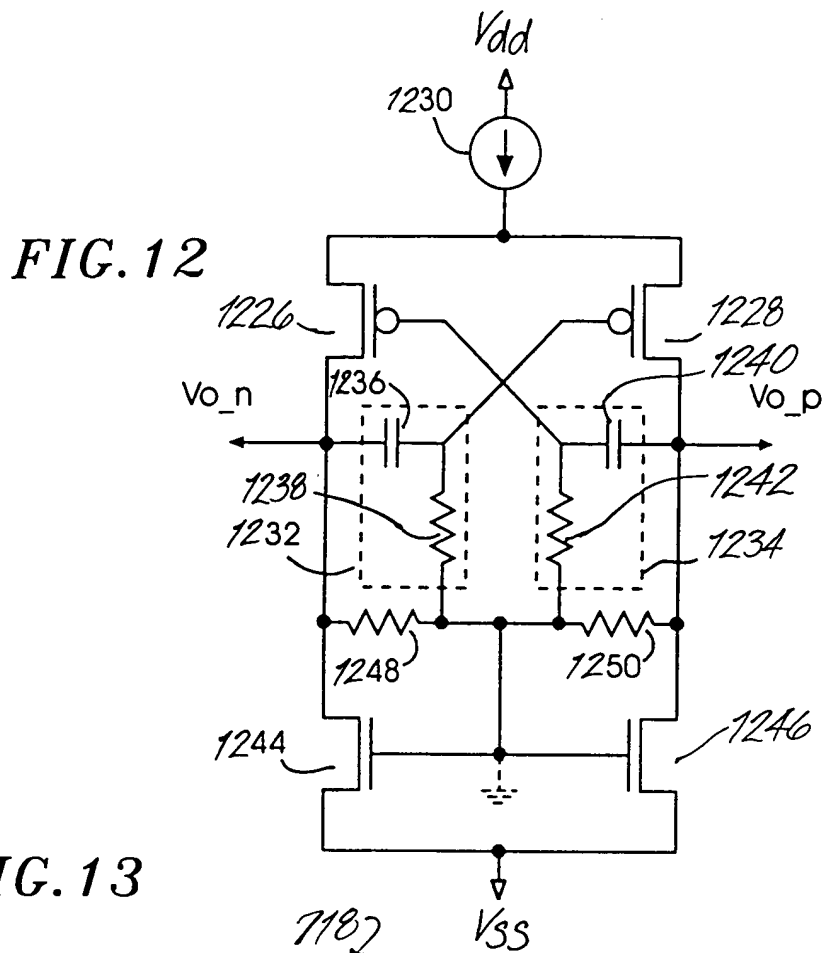
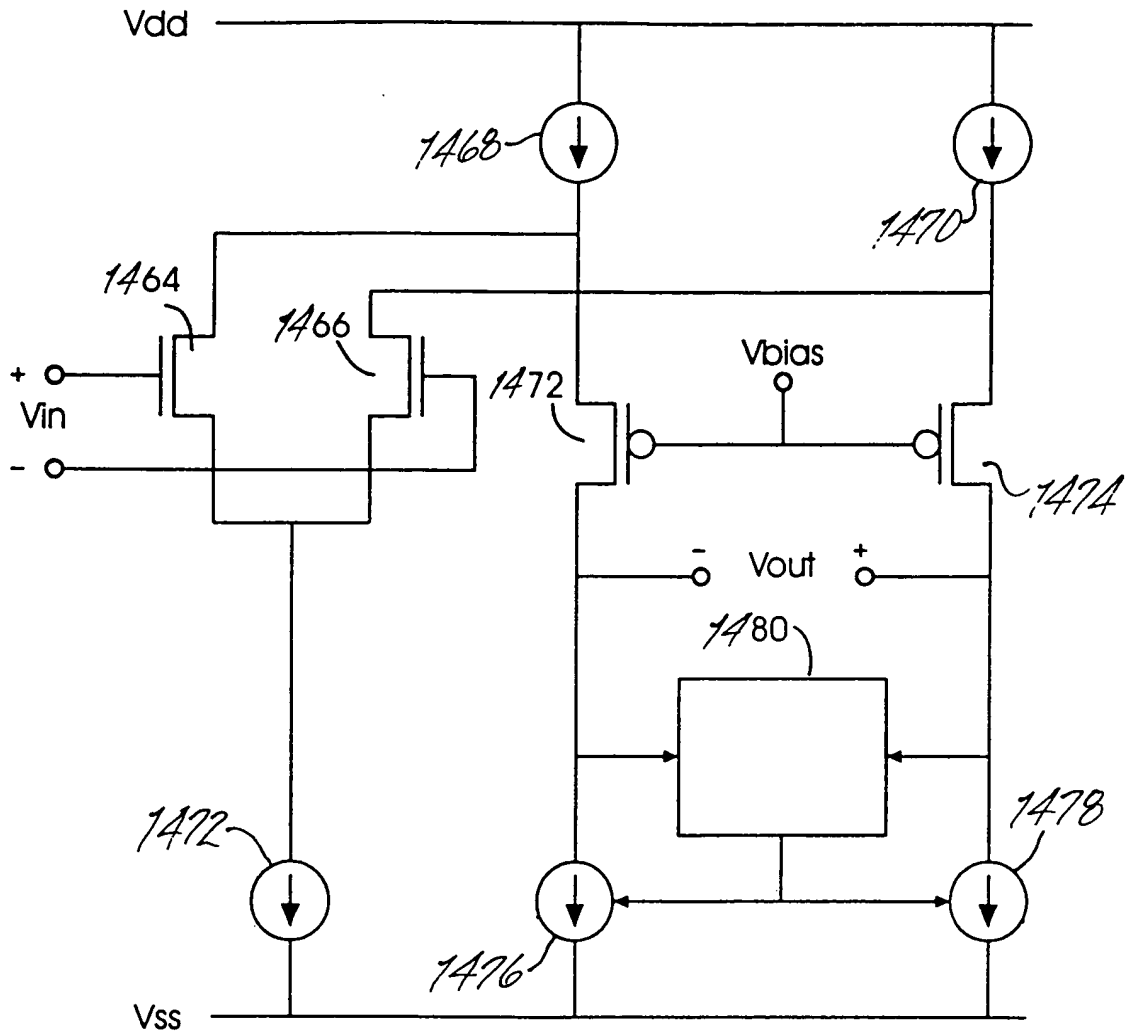


FIG. 14



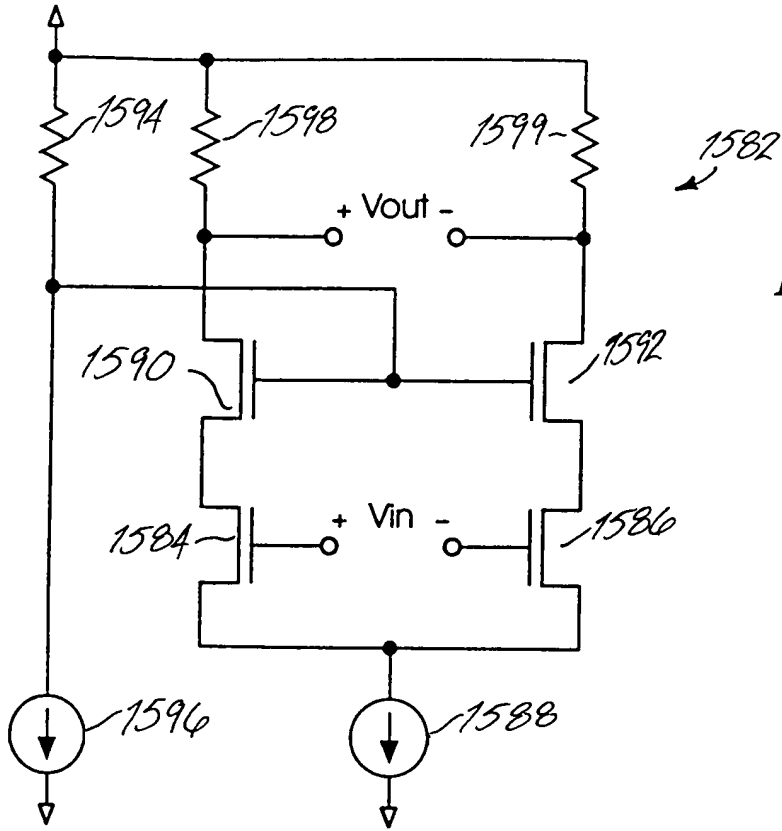
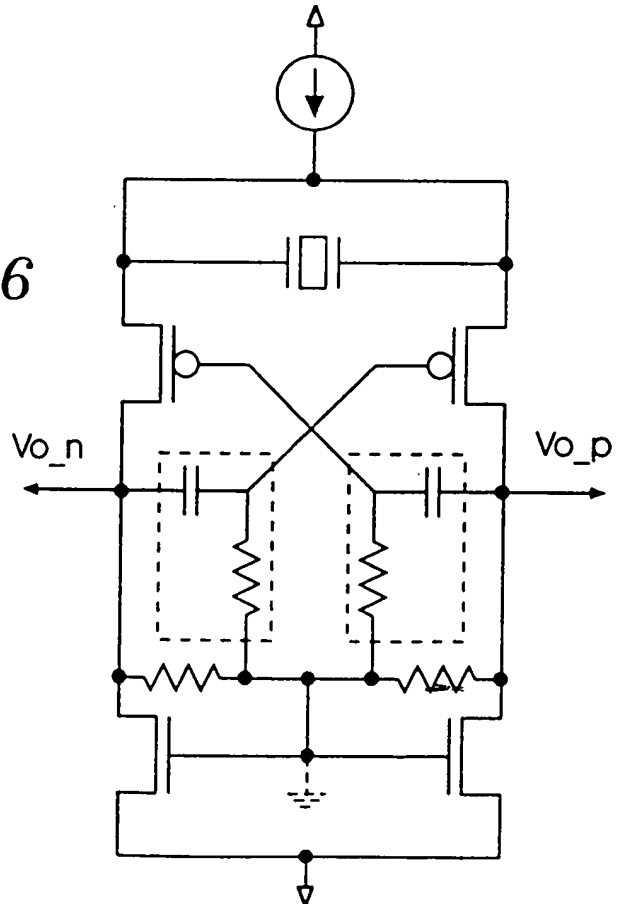


FIG. 15

FIG. 16



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FIG. 17

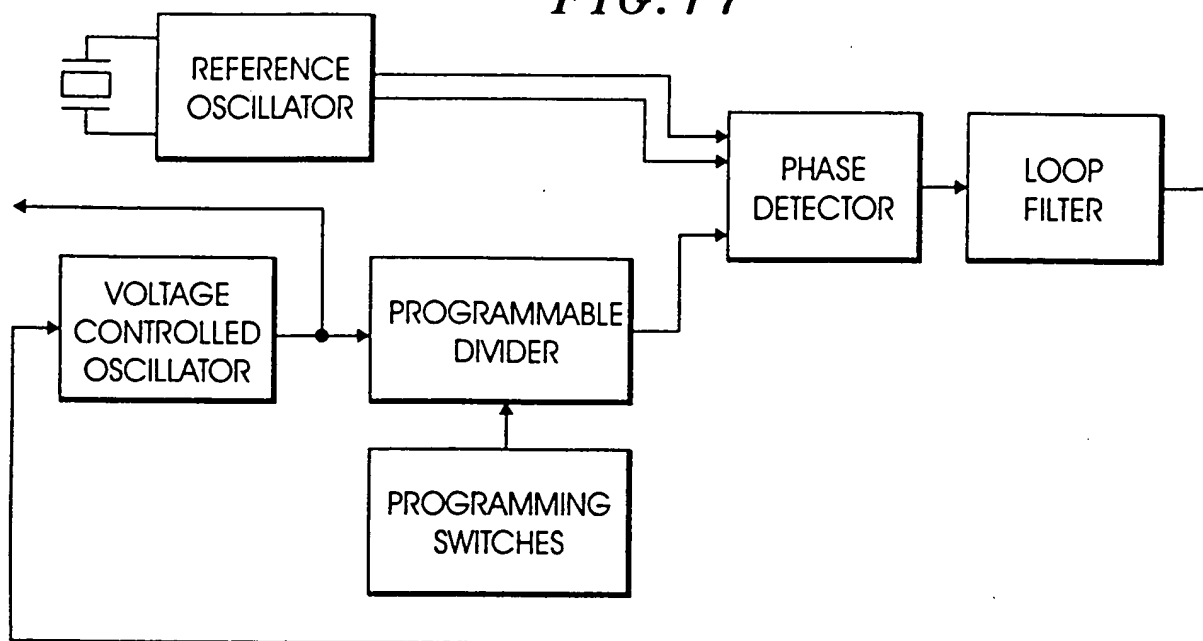


FIG. 18

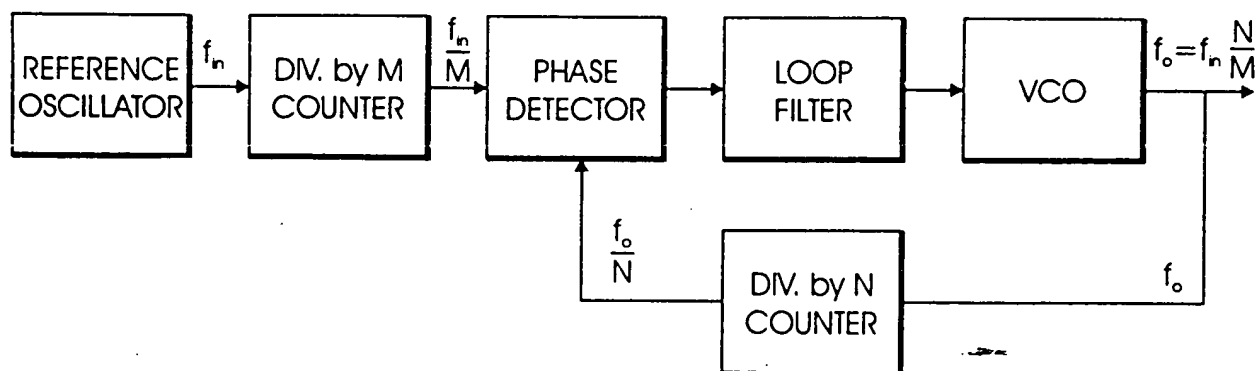


FIG. 19

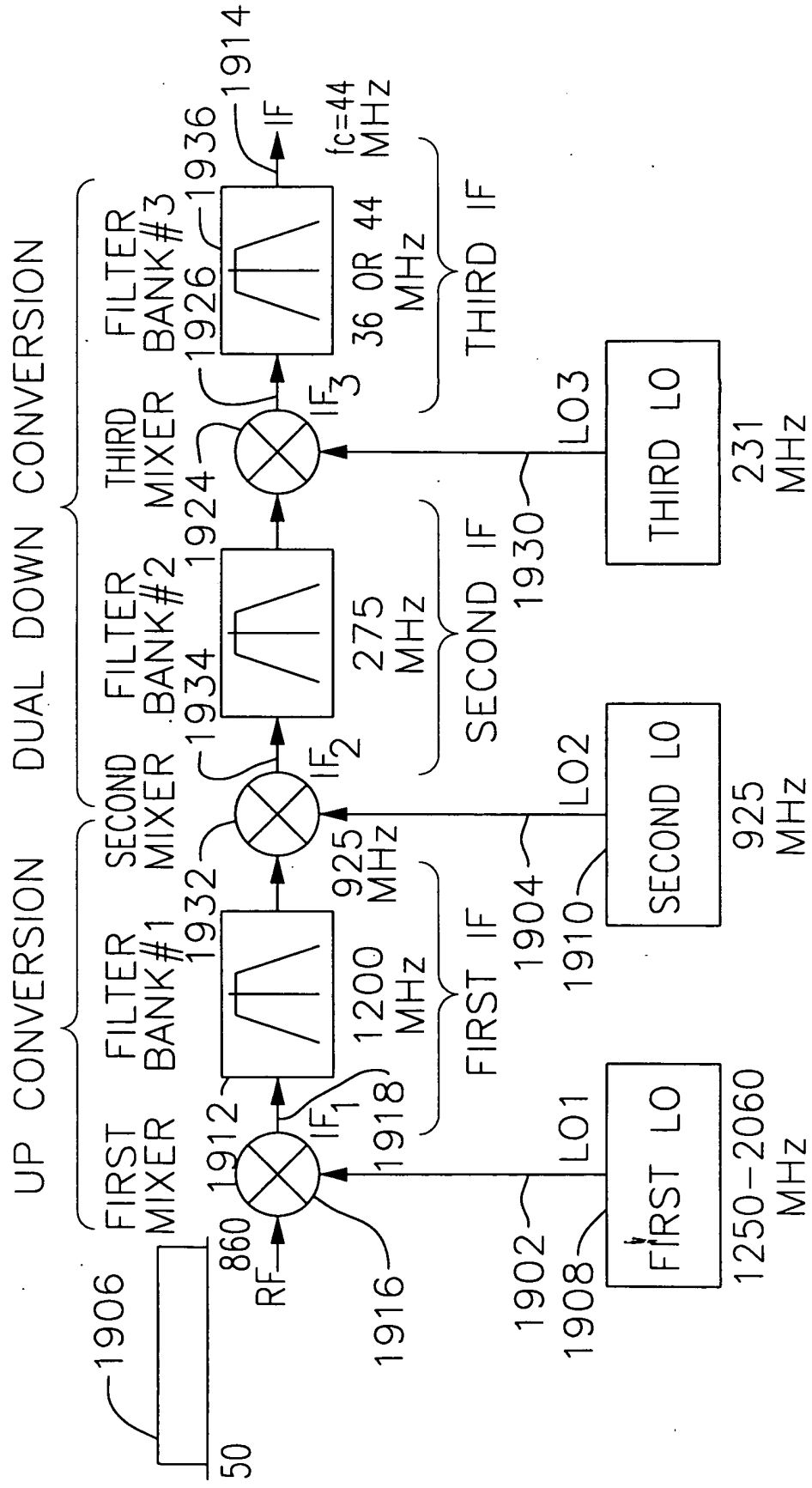


FIG. 20

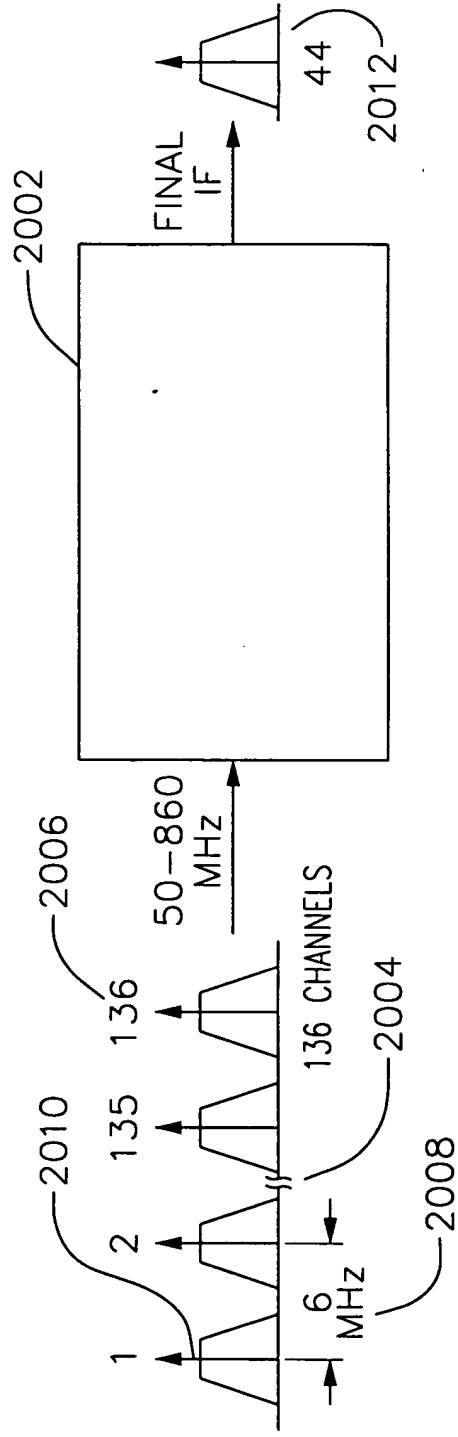


FIG. 21

PPL Xtol REFERENCE=10MHz
 LO-1, 10MHz FREQUENCY STEPS
 LO-2, 100kHz FREQUENCY STEPS

44MHz IF

NOTE
 • LO-2 REF=100KHz,
 SO DIVIDE RANGE=9216 TO 9280

TABLE OF FREQUENCIES BASED ON
 COARSE/FINE PLL SOLUTION:

Frq (MHz)	50	56	62	68	74	80	86	92	98	104	110	116	122	128	"	854	860
LO-1(MHz)	1250	1260	1260	1270	1270	1280	1290	1290	1300	1300	1310	1320	1320	1330	"	2050	2060
IF-1 (MHz)	1200	1204	1198	1202	1196	1200	1204	1198	1202	1196	1200	1204	1198	1202	"	1196	1200
LO-2(MHz)	924.8	928.0	923.2	926.4	921.6	924.8	928.0	923.2	926.4	921.6	924.8	928.0	923.2	926.4	"	921.6	924.8
IF-2(MHz)	275.2	276.0	274.8	275.6	274.4	275.2	276.0	274.8	275.6	274.4	275.2	276.0	274.8	275.6	"	274.4	275.2
LO-3(MHz)	231.2	232	230.8	232	230	231	232	231	232	230	231	232	231	232	"	230	231
IF-3(MHz)	44.0	44.0	44.0	44.0	44.0	44.0	44.0	44.0	44.0	44.0	44.0	44.0	44.0	44.0	"	44.0	44.0

FIG.22

PPL Xtol REFERENCE=10MHz
 LO-1, 10MHz FREQUENCY STEPS
 LO-2, 100kHz FREQUENCY STEPS

36MHz IF

NOTE
 • LO-2 REF=100KHz,
 SO DIVIDE RANGE=9280 TO 9340

TABLE OF FREQUENCIES BASED ON
 COARSE/FINE PLL SOLUTION:

Fr1 (MHz)	50	58	66	74	82	90	98	106	114	122	130	138	146	154	"	852	860
LO-1(MHz)	1250	1260	1270	1270	1280	1290	1300	1310	1310	1320	1330	1340	1350	1350	"	2050	2060
IF-1 (MHz)	1200	1202	1204	1196	1198	1200	1202	1204	1196	1198	1200	1202	1204	1196	"	1198	1200
LO-2(MHz)	931.2	932.8	934.4	928.0	930	931	933	934	928.0	930	931	933	934	928.0	"	929.60	931.2
IF-2(MHz)	268.8	269.2	269.6	268.0	268.4	268.8	269.2	269.6	268.0	268.4	268.8	269.2	269.6	268.0	"	268.4	268.8
LO-3(MHz)	232.8	233.2	233.6	232	232	233	233	234	232	232	233	233	234	232.0	"	232.4	232.8
IF-3(MHz)	36.0	36.0	36.0	36.0	36.0	36.0	36.0	36.0	36.0	36.0	36.0	36.0	36.0	36.0	"	36.0	36.0

FIG. 23

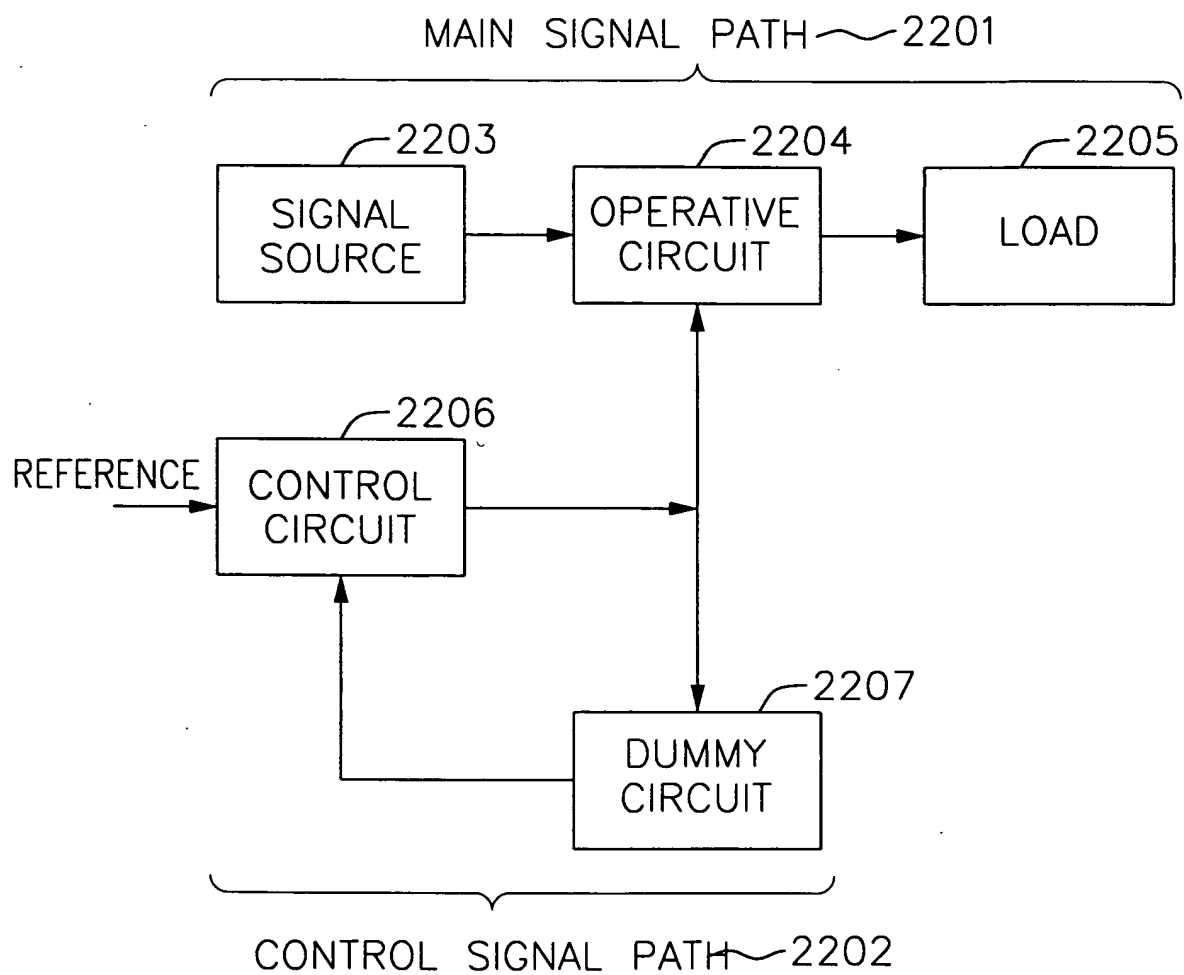
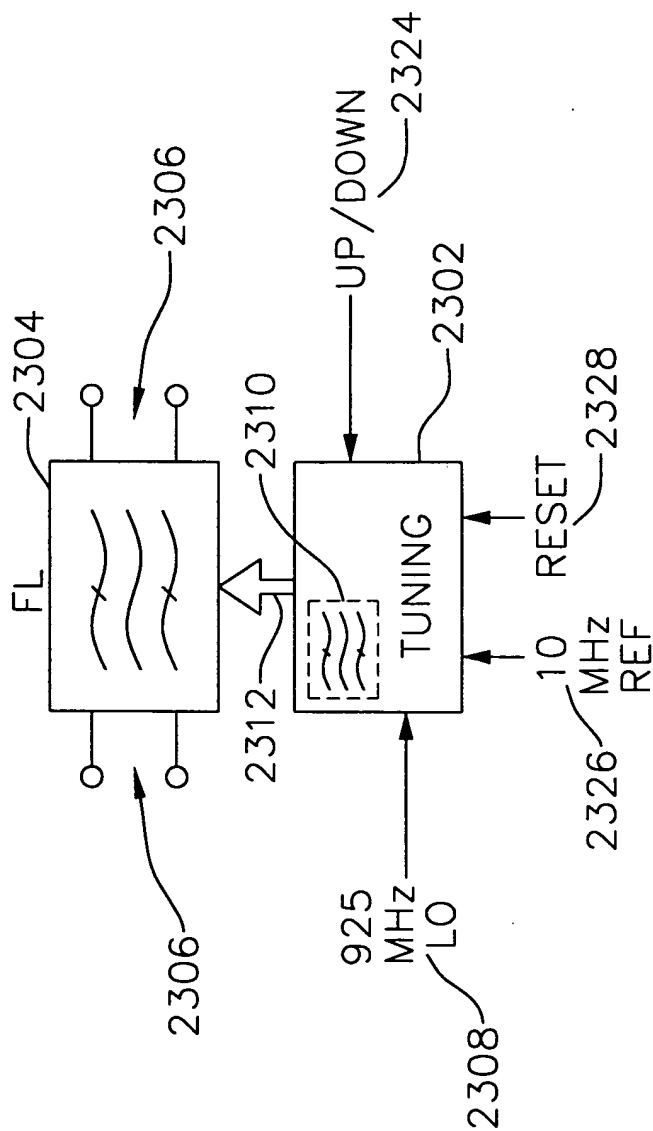


FIG. 23

FIG. 24a



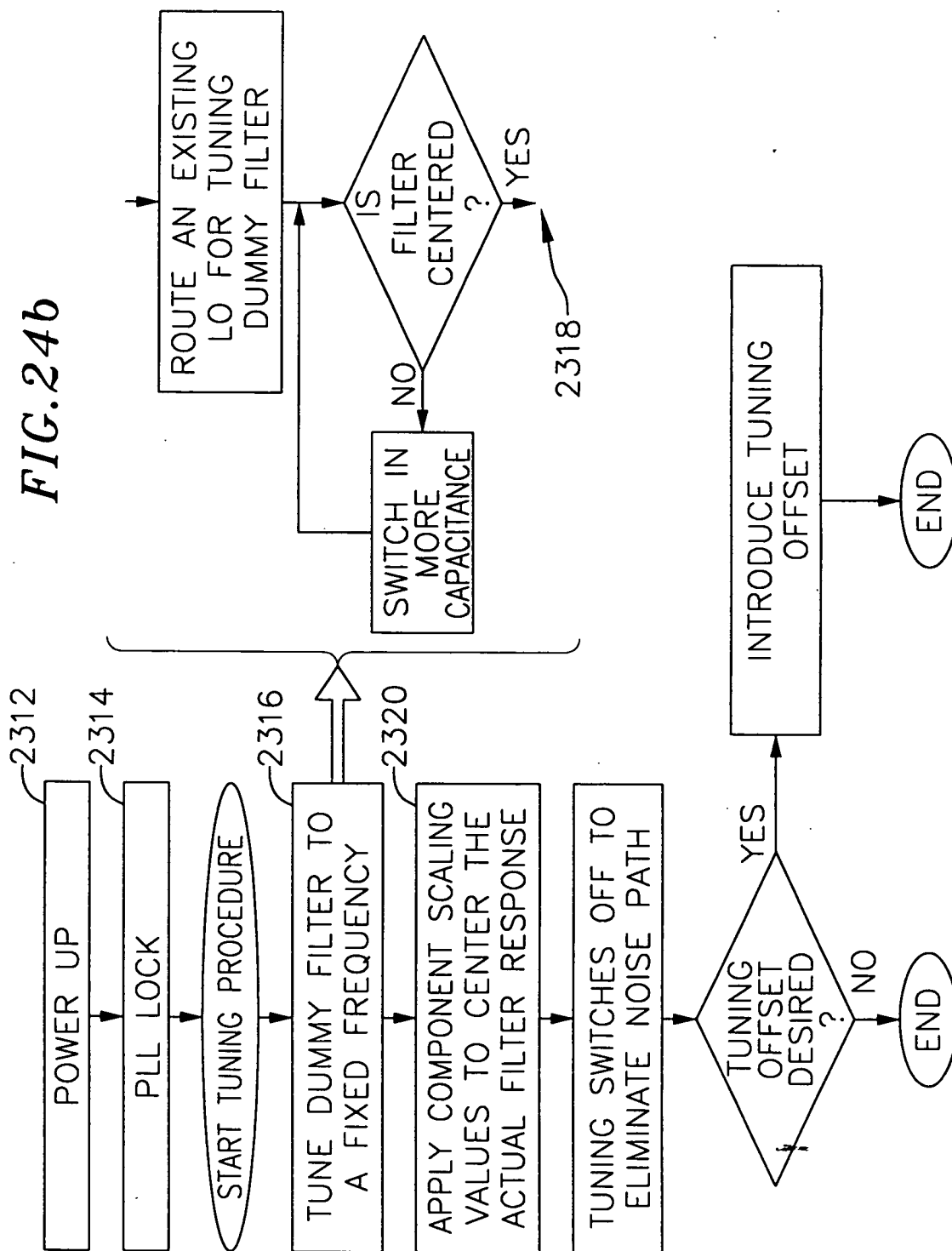


FIG. 24c

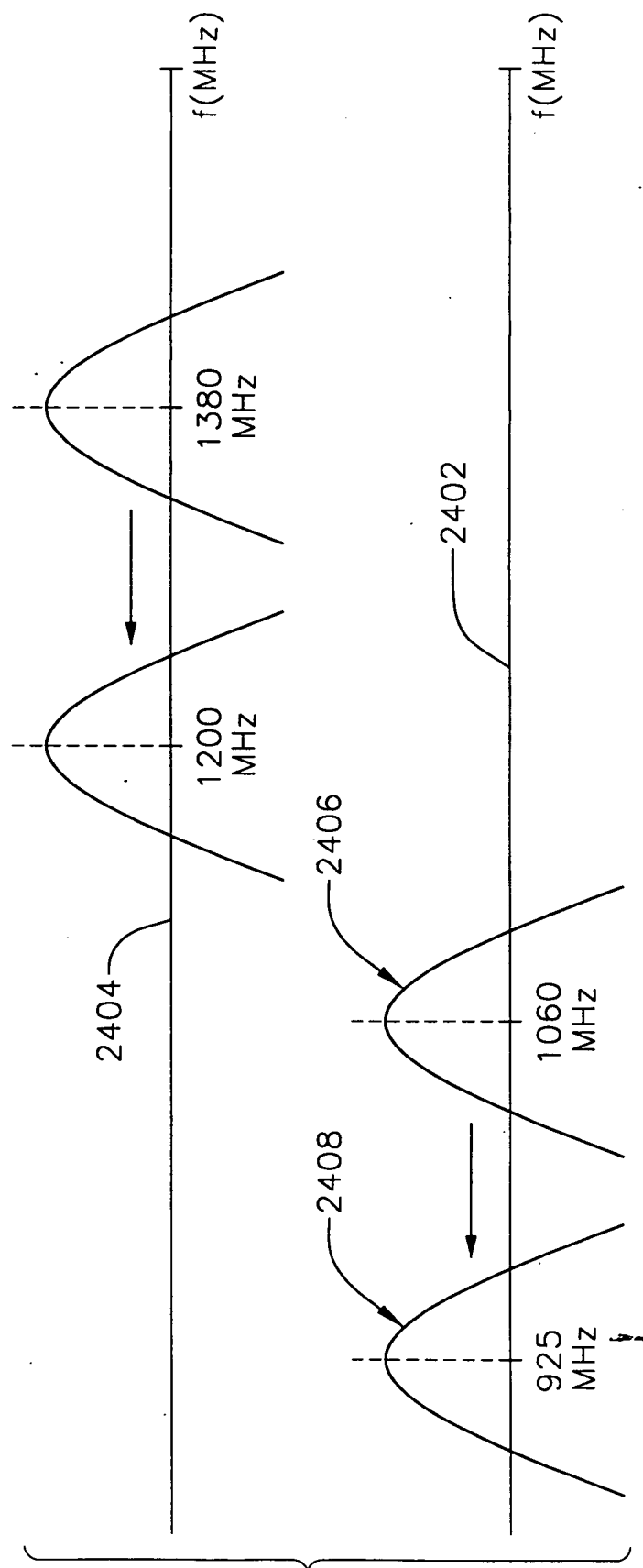


FIG. 25

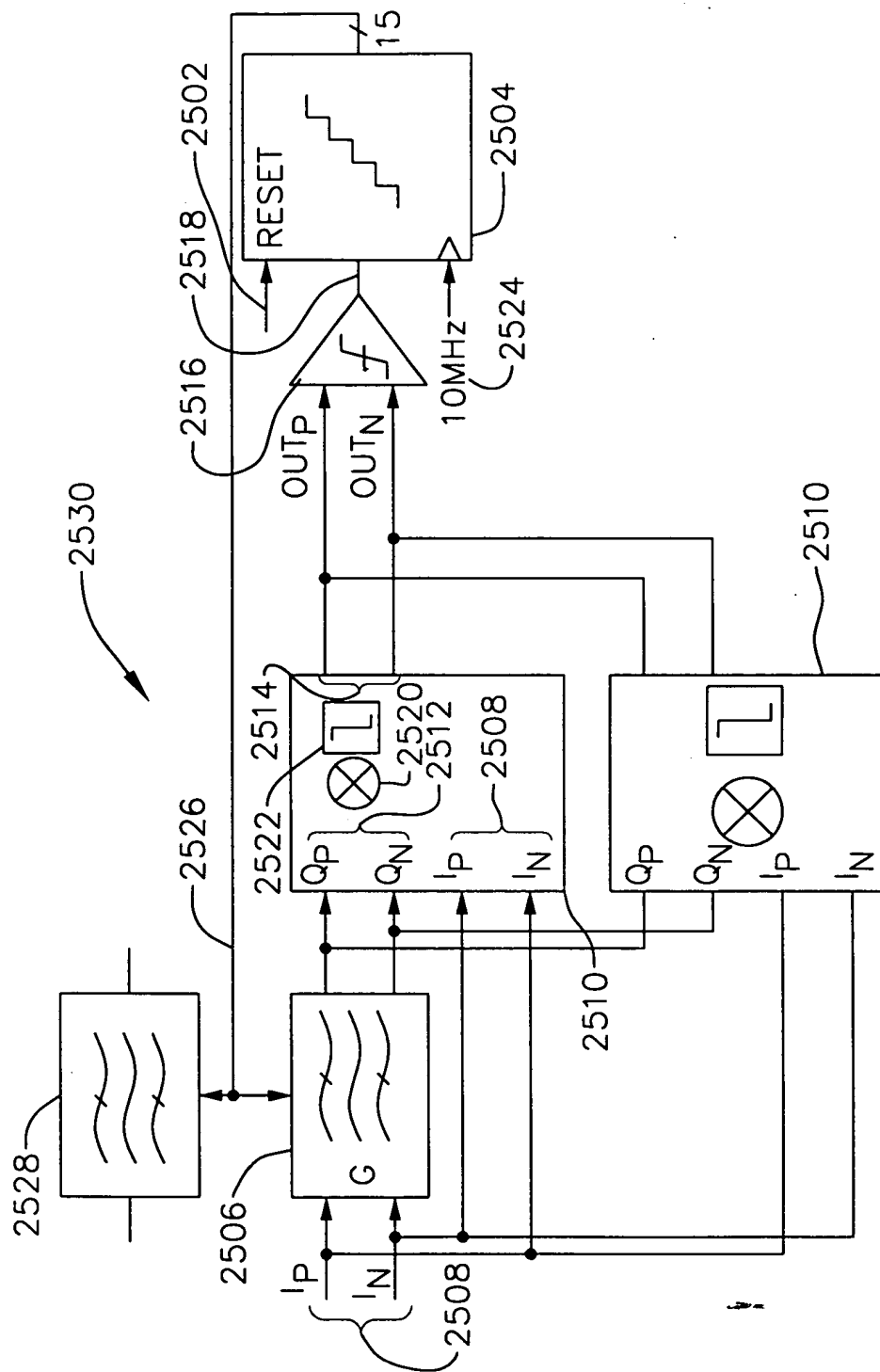
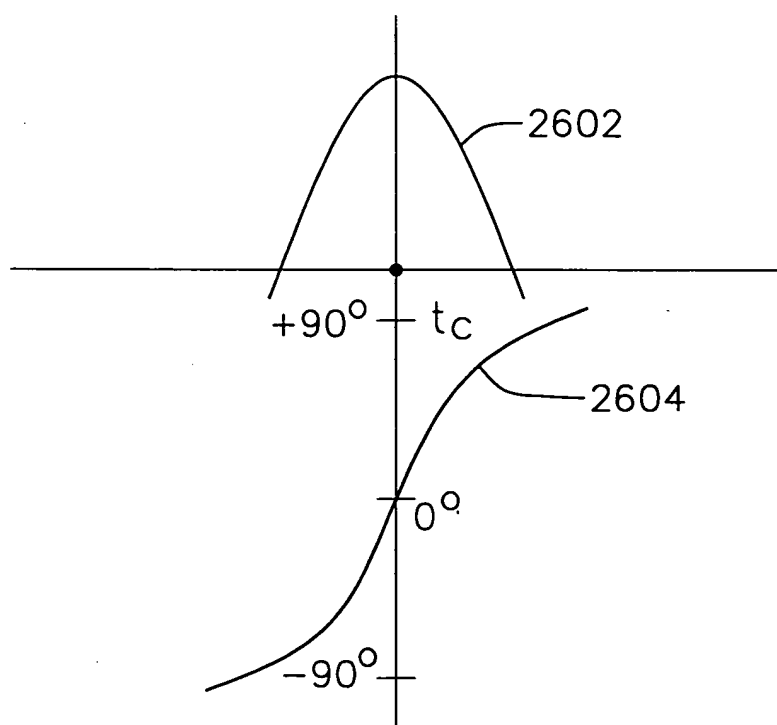
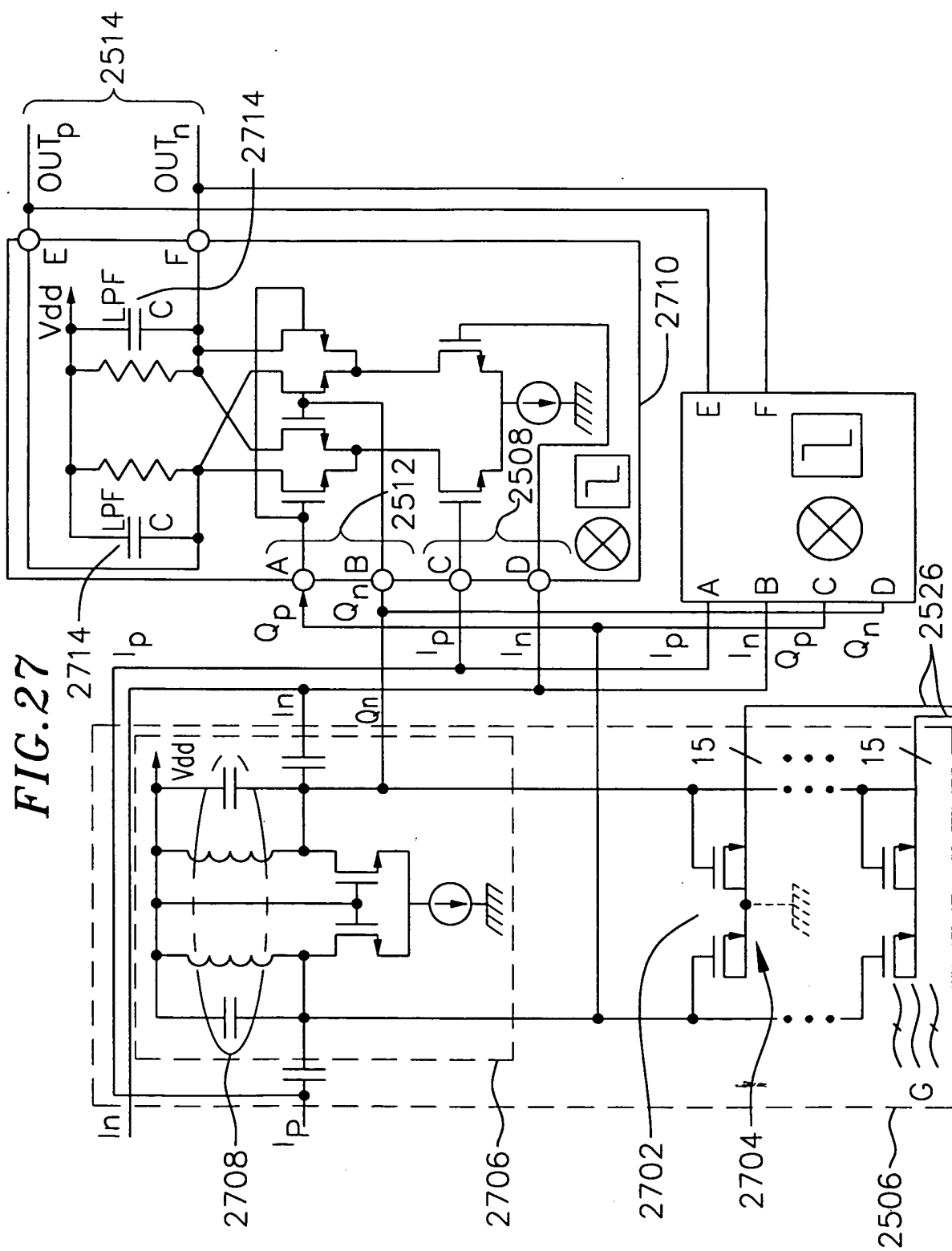


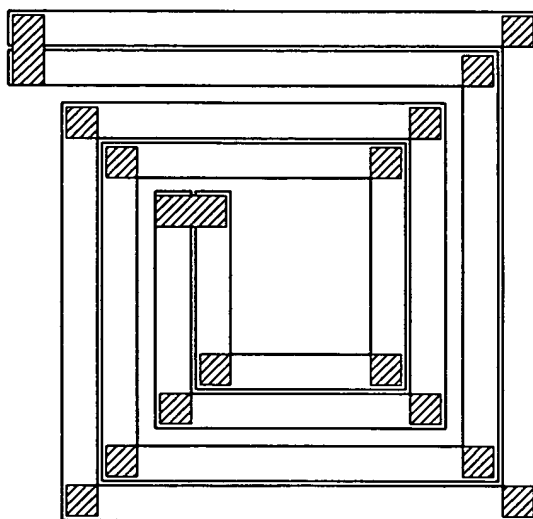
FIG.26





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FIG.28



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FOOT-84099260

FIG.29

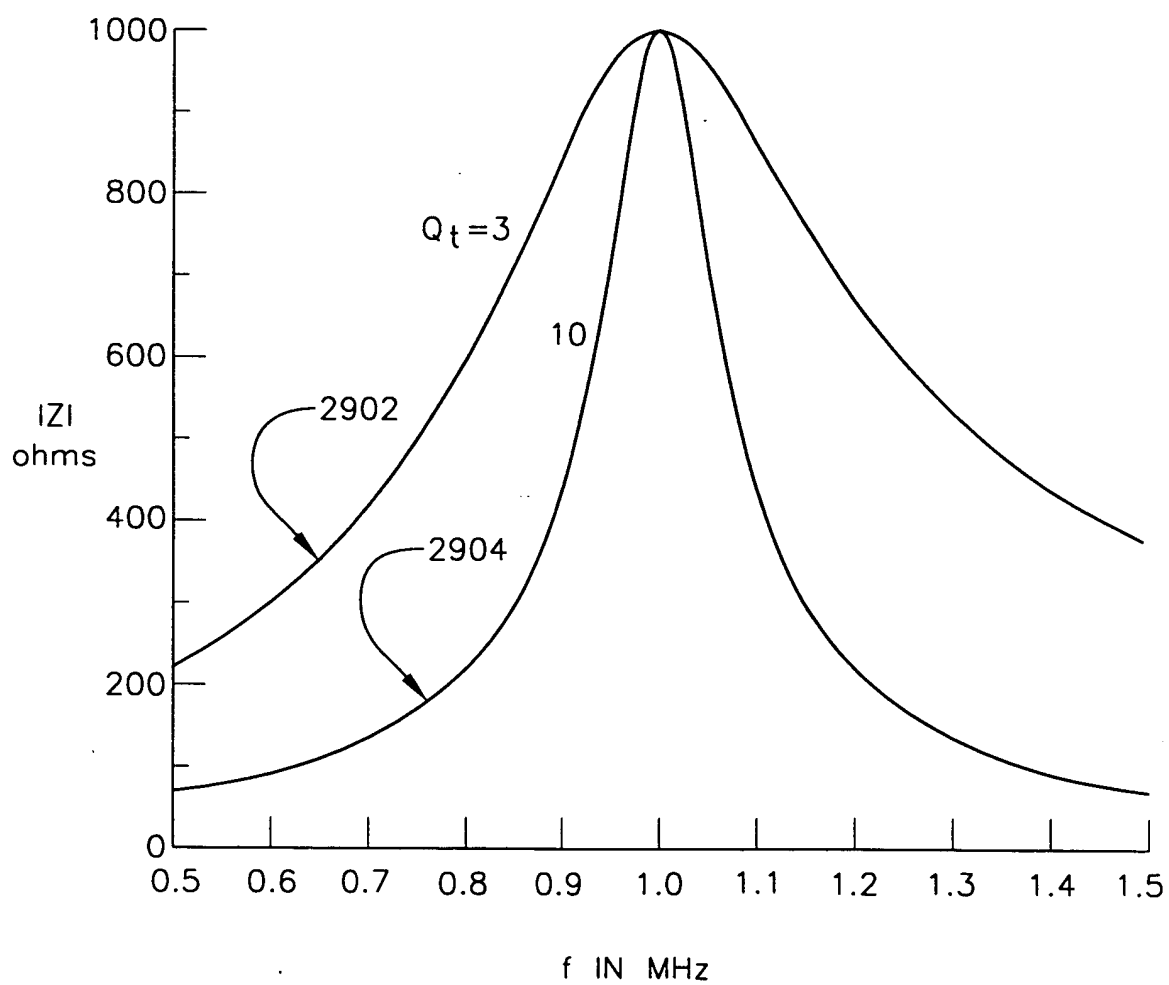


FIG. 30

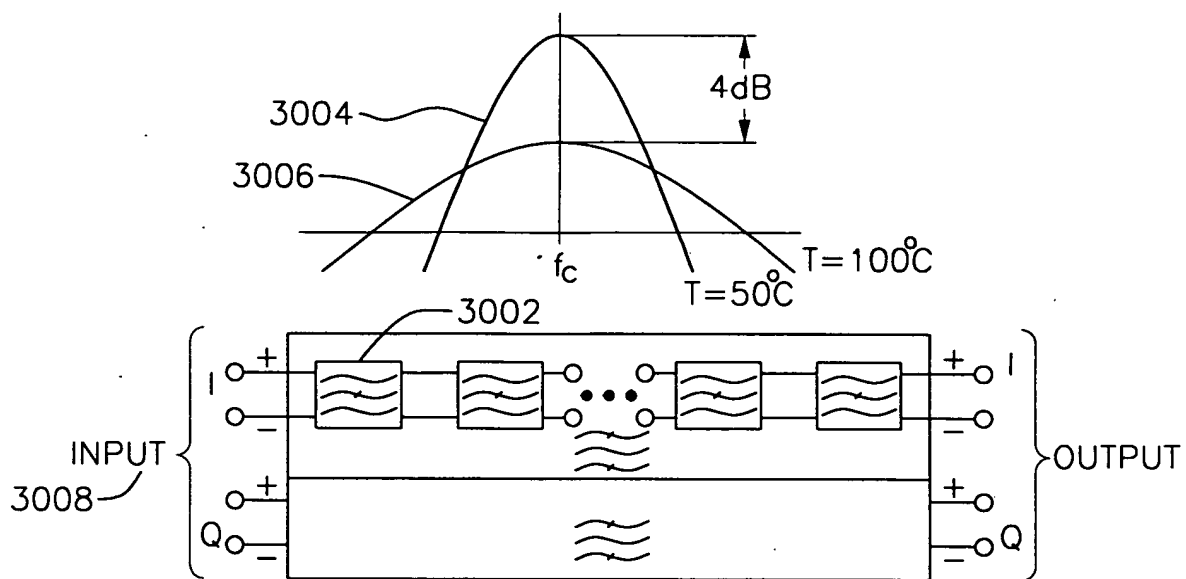


FIG. 31

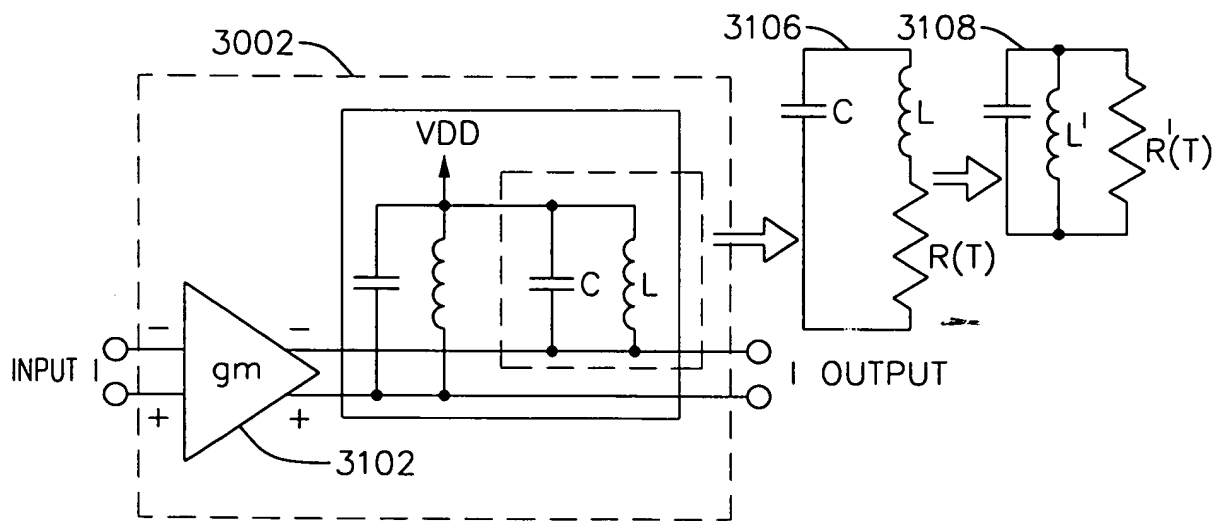


FIG. 33

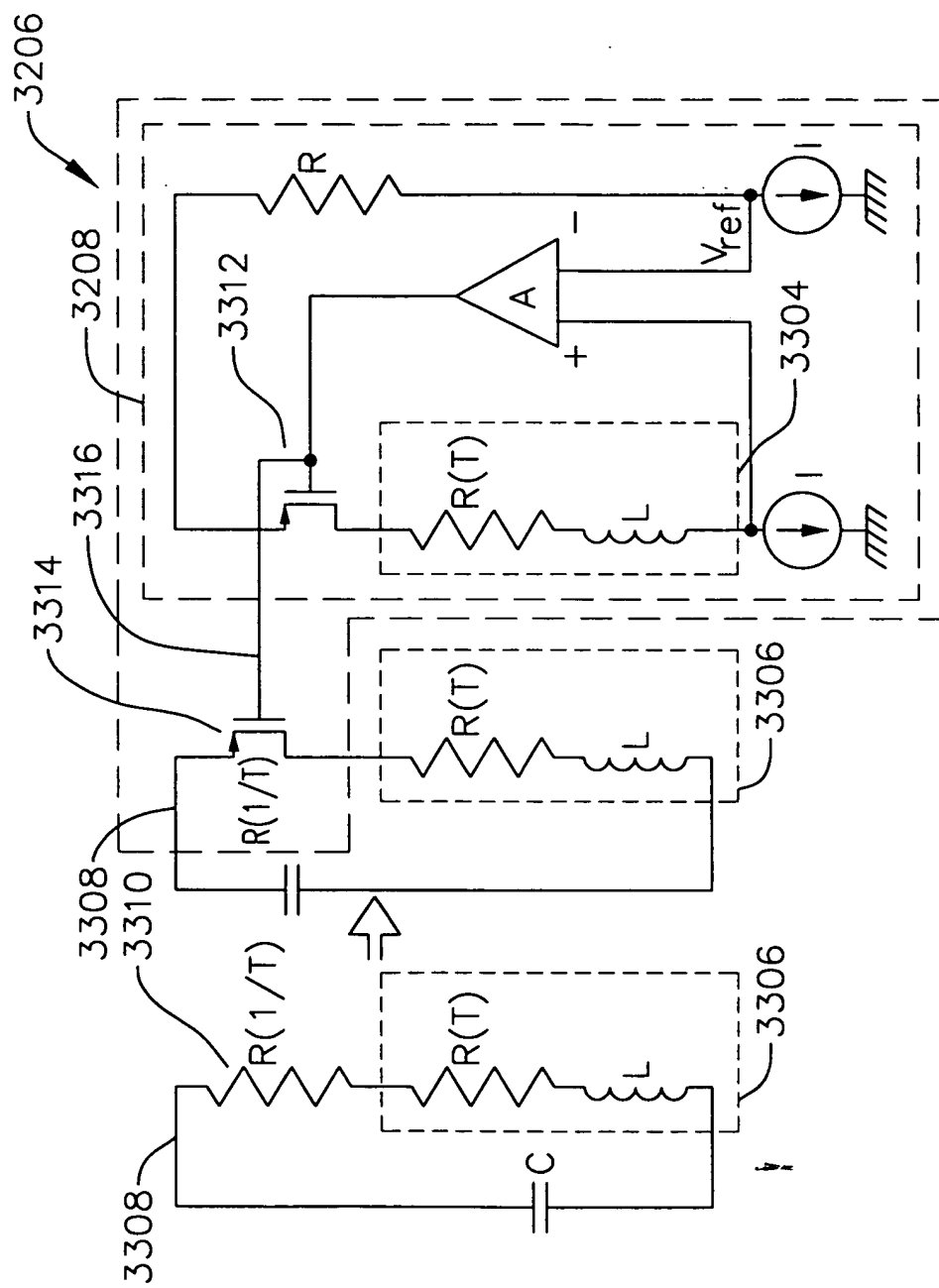


FIG.34

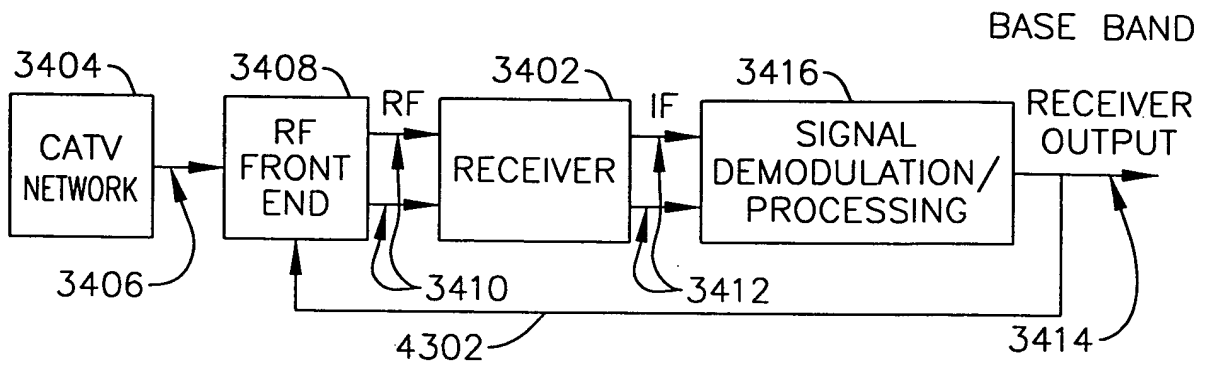


FIG.35

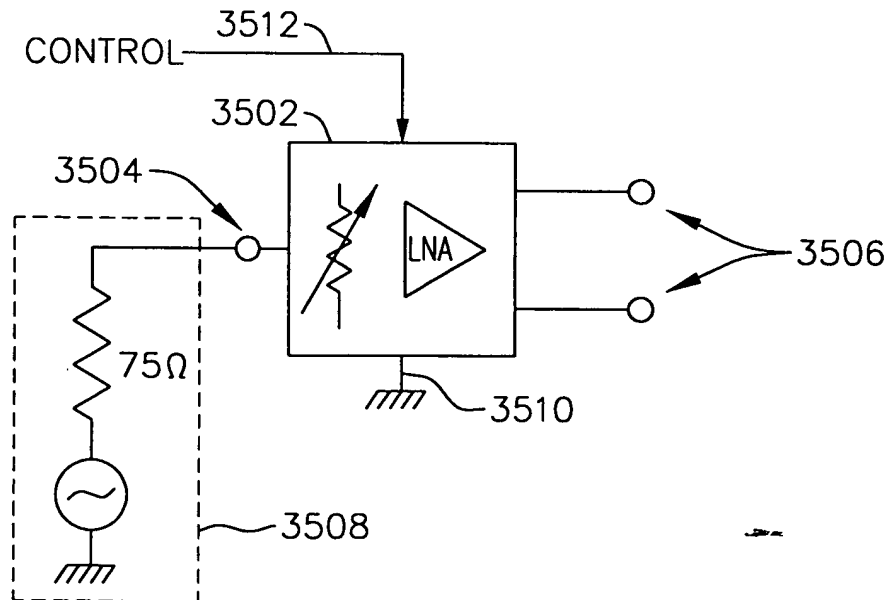


FIG. 37

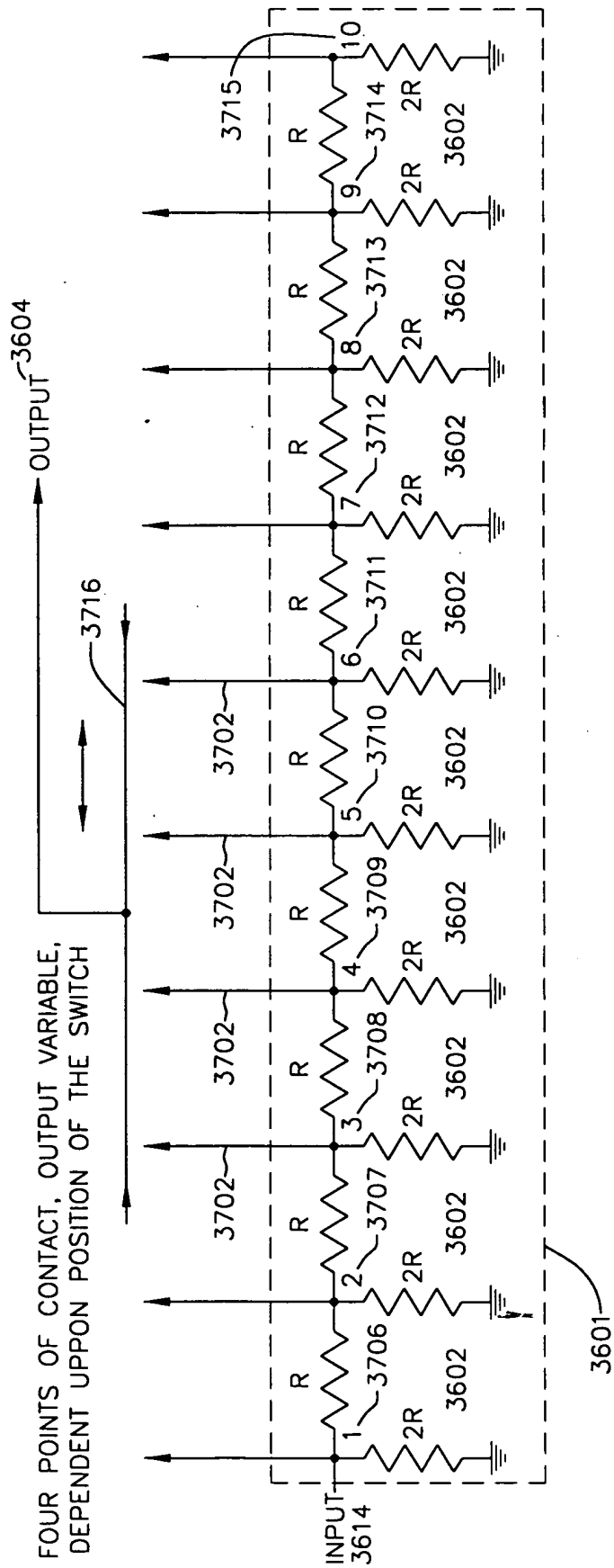


FIG. 38

PGA SETTINGS

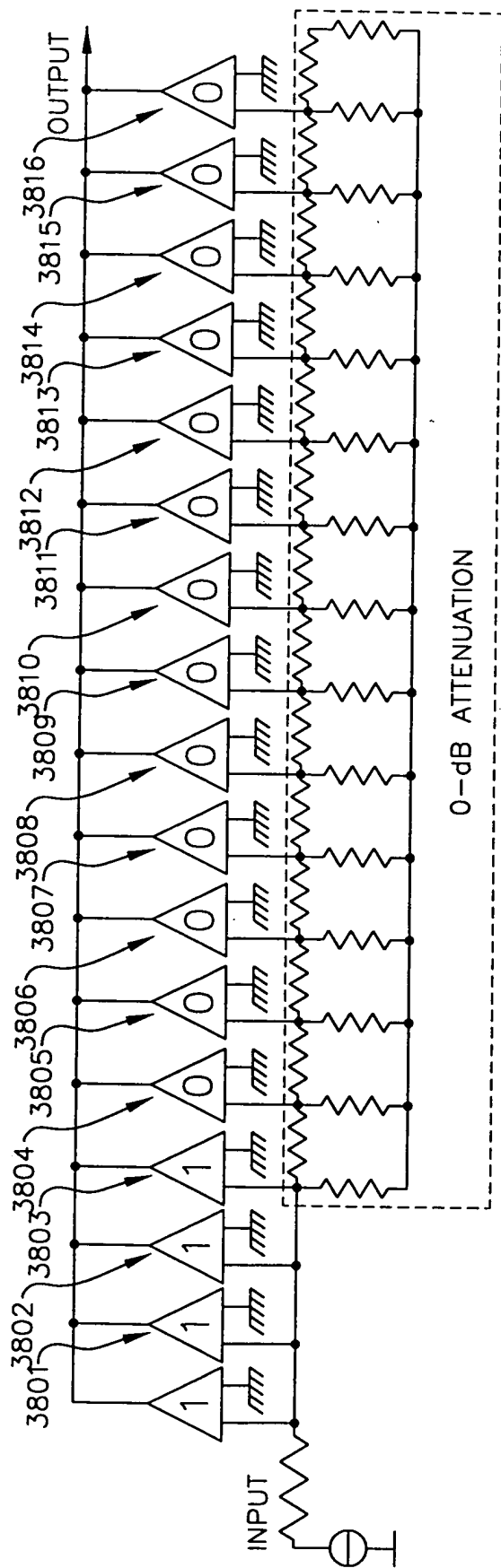


FIG.39

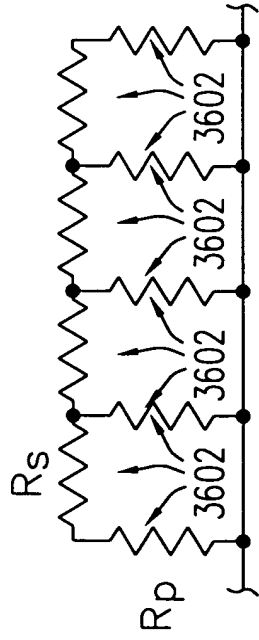


FIG.40

PGA ARCHITECTURE

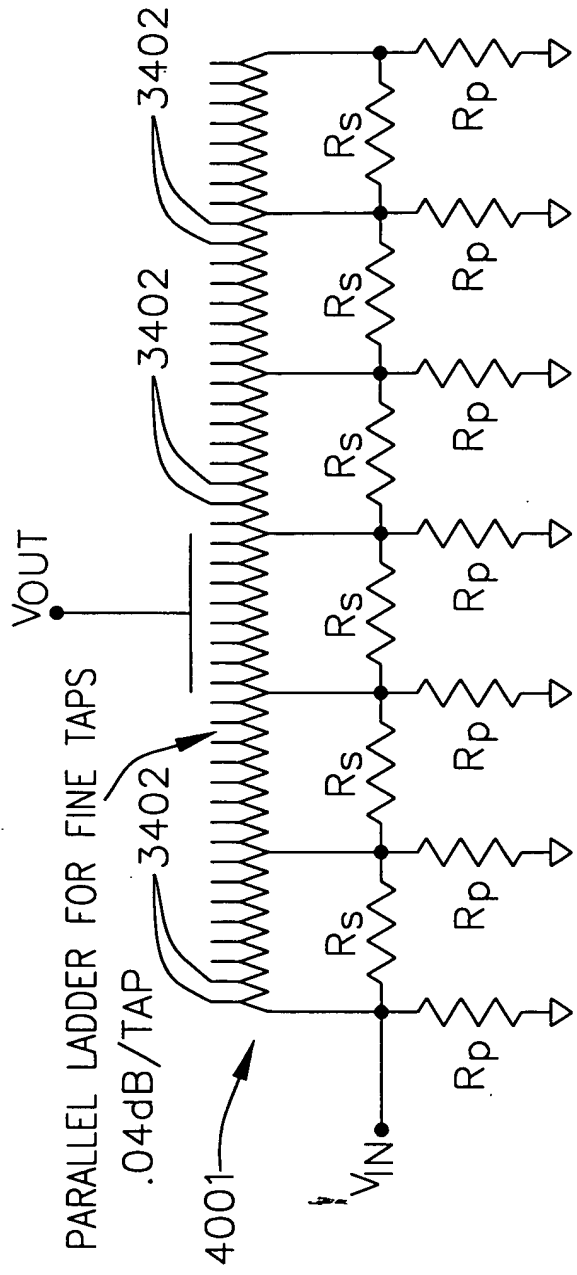


FIG. 41

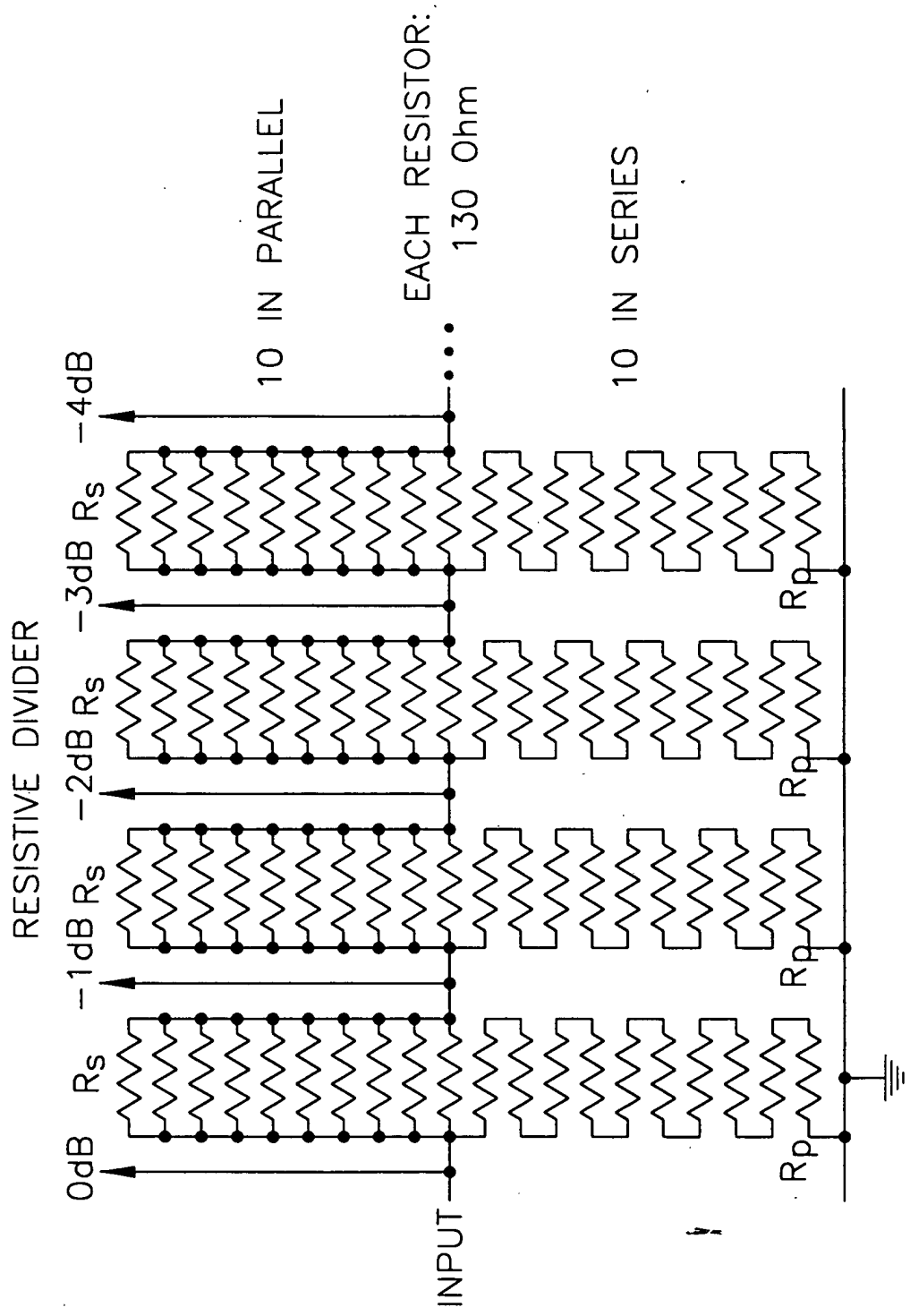
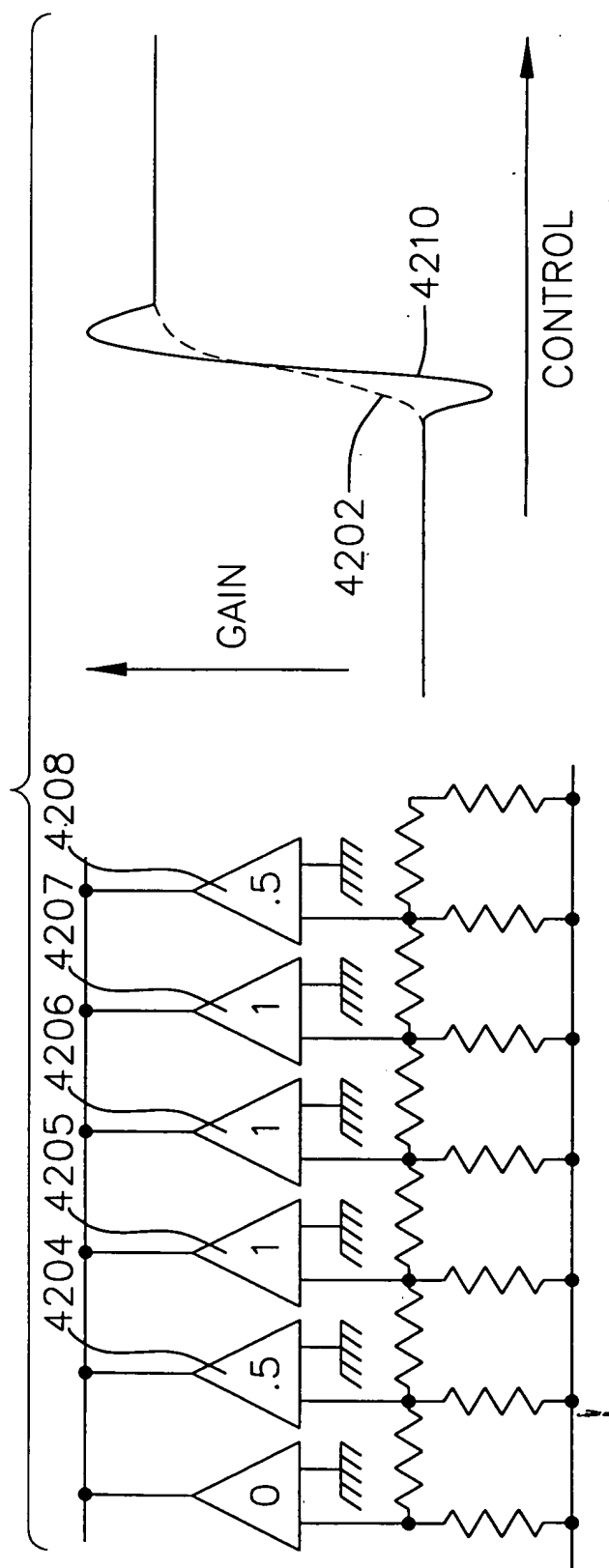


FIG. 42

NON-MONOTONICITY



CLAMPING CONTROL RANGE

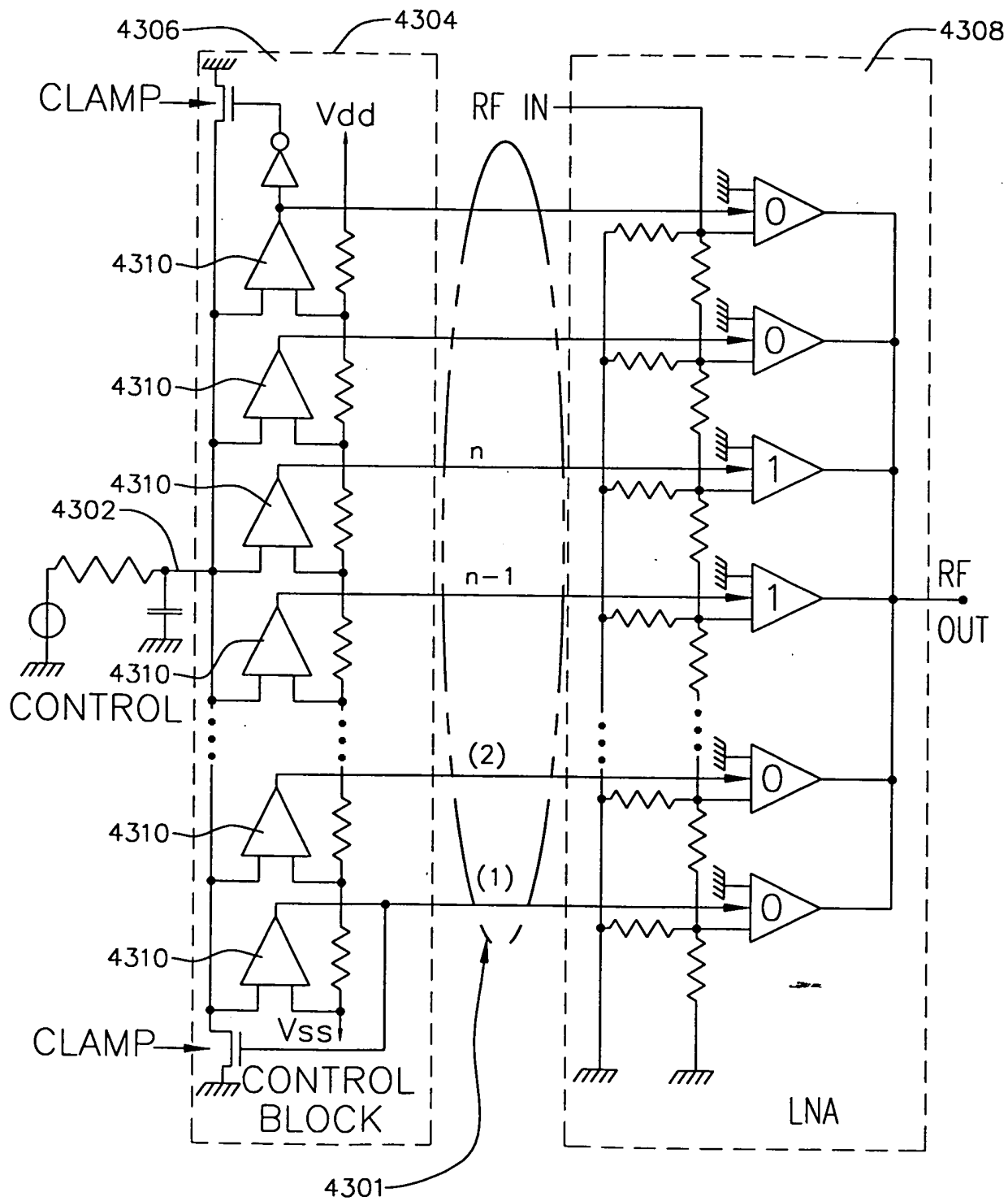


FIG. 44a
CONTROLLED GAIN COMPARATOR

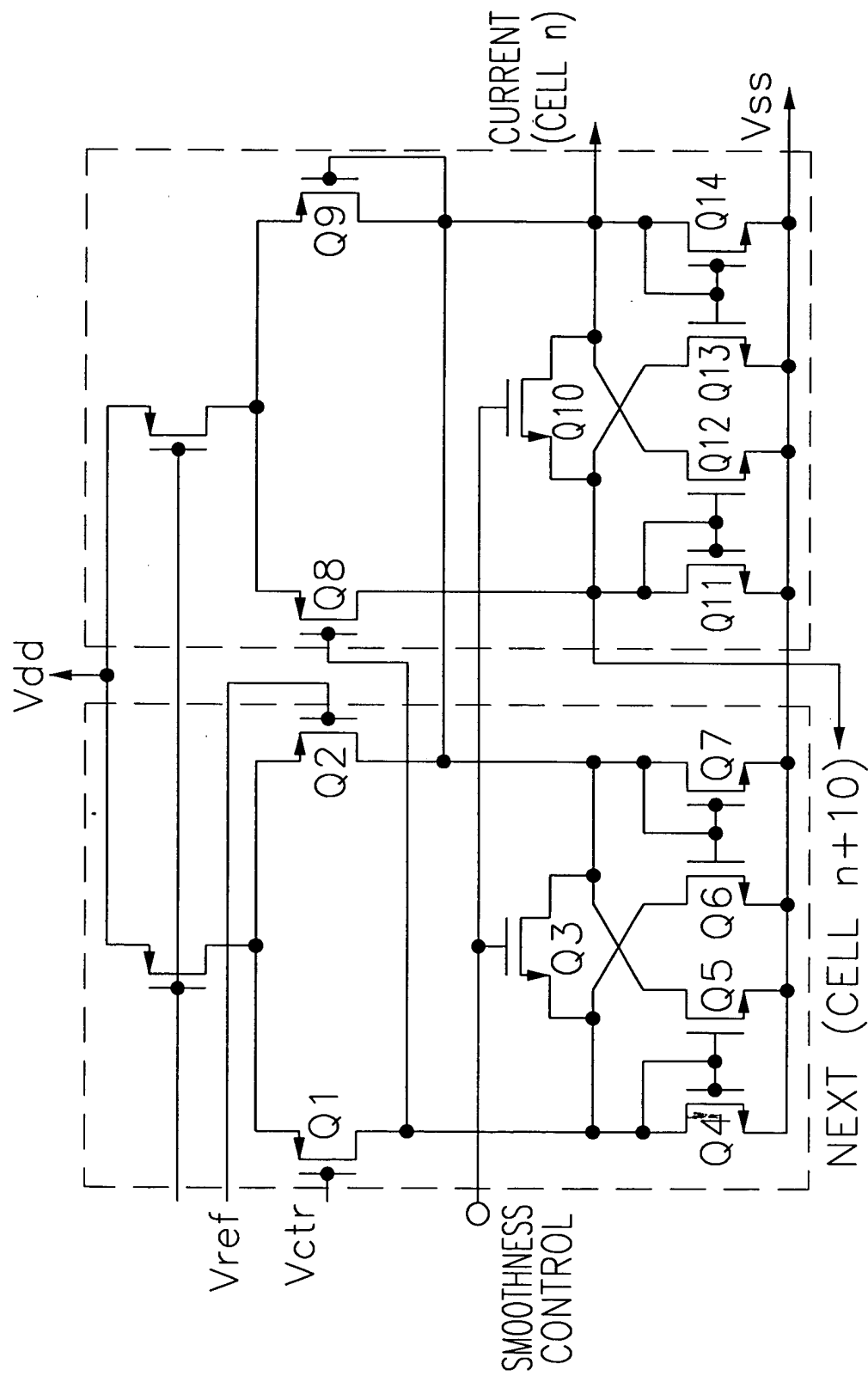
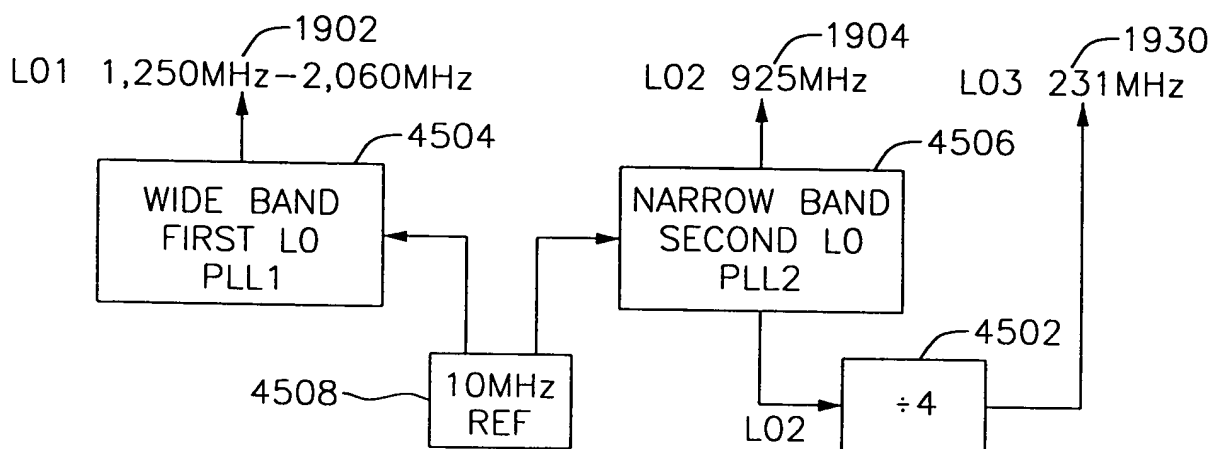


FIG. 45



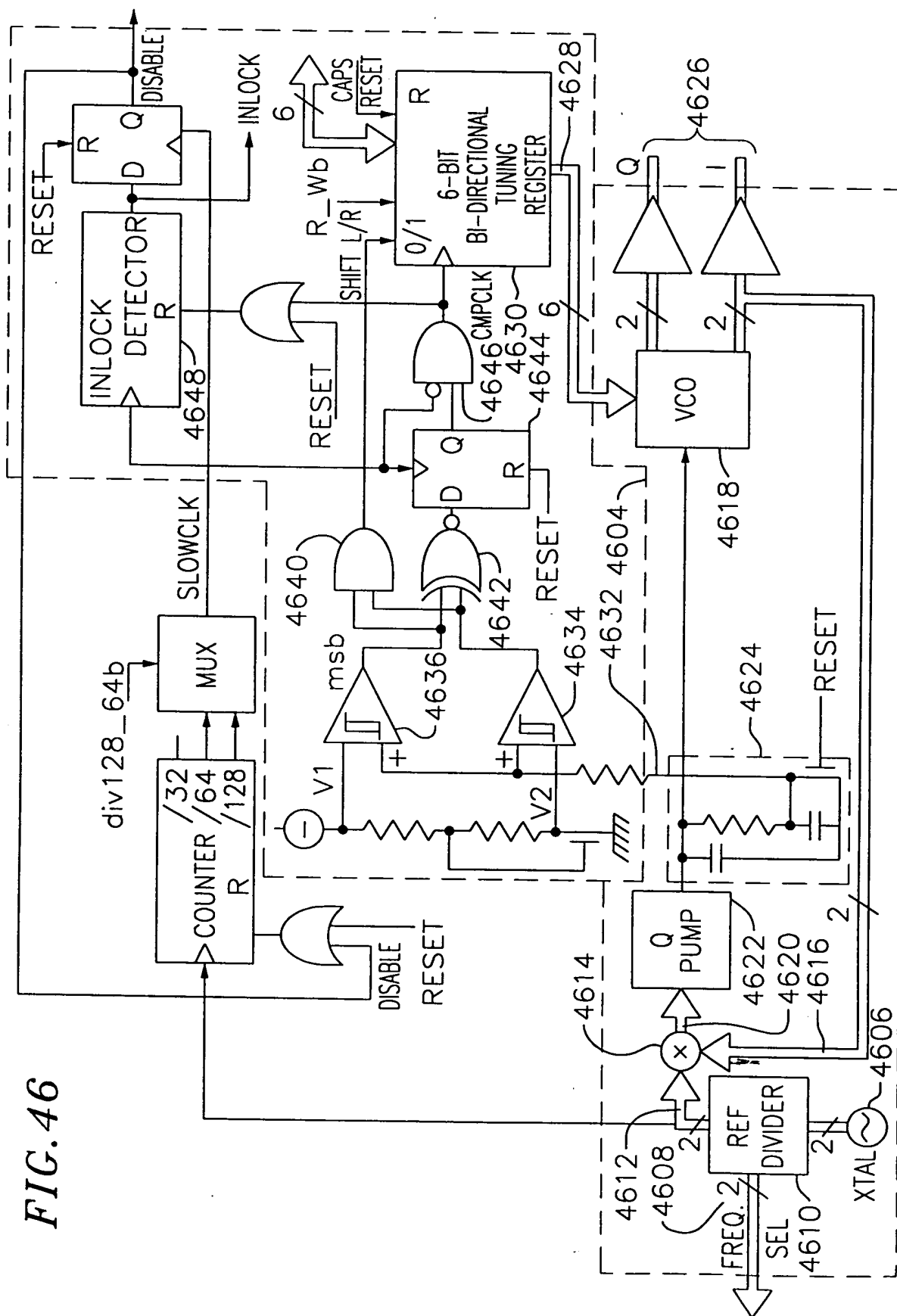


FIG. 47

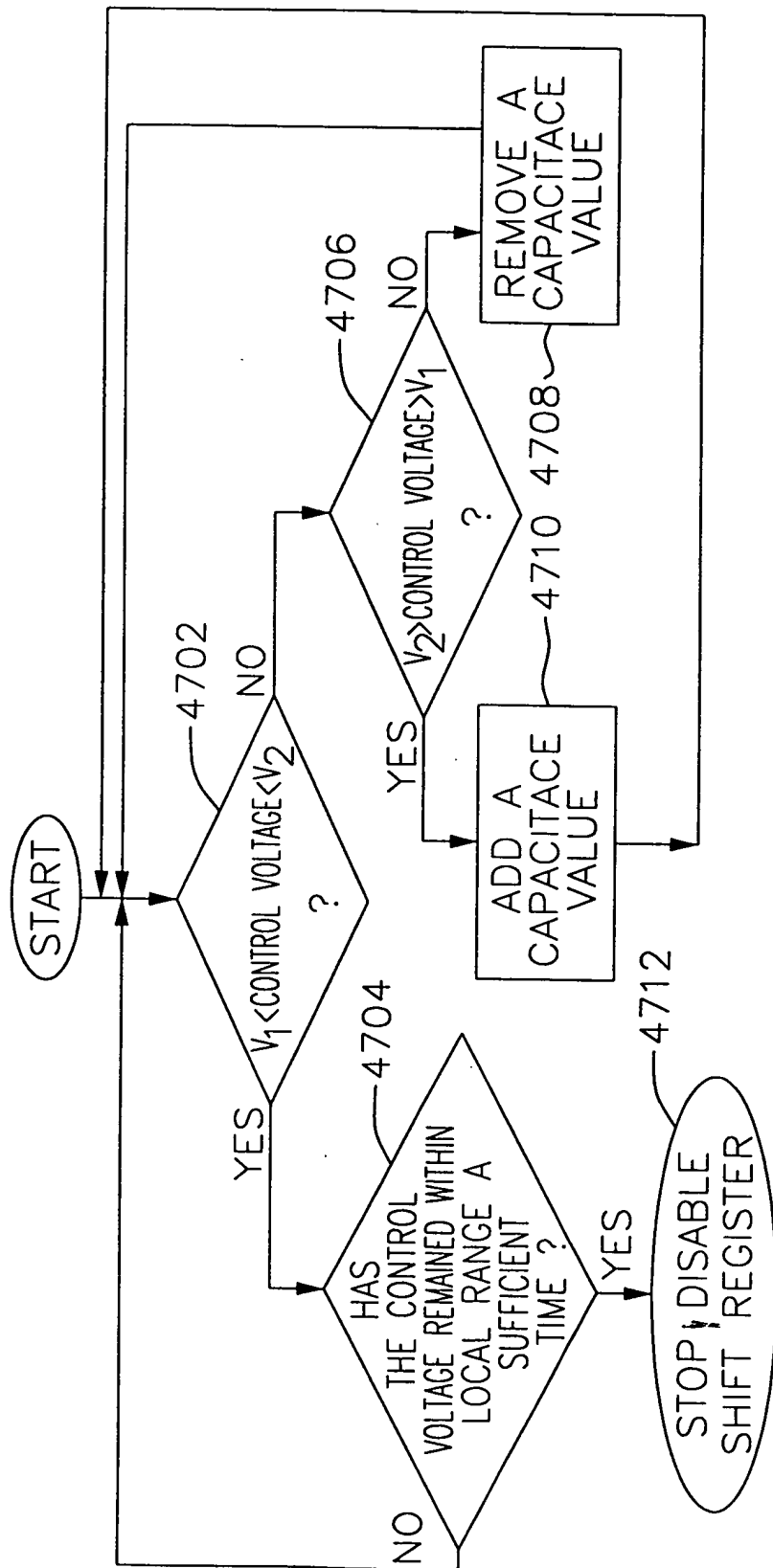
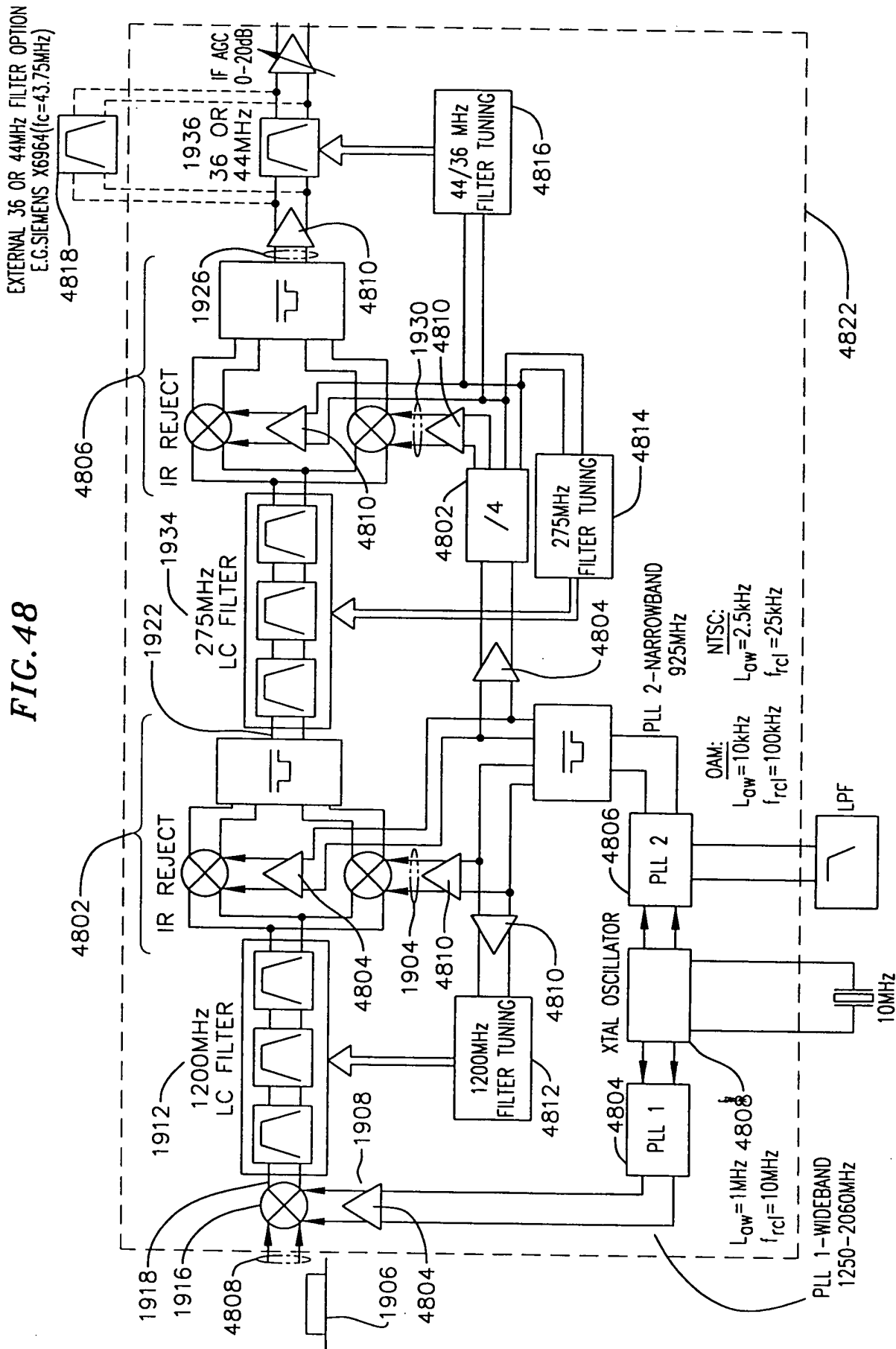


FIG. 48



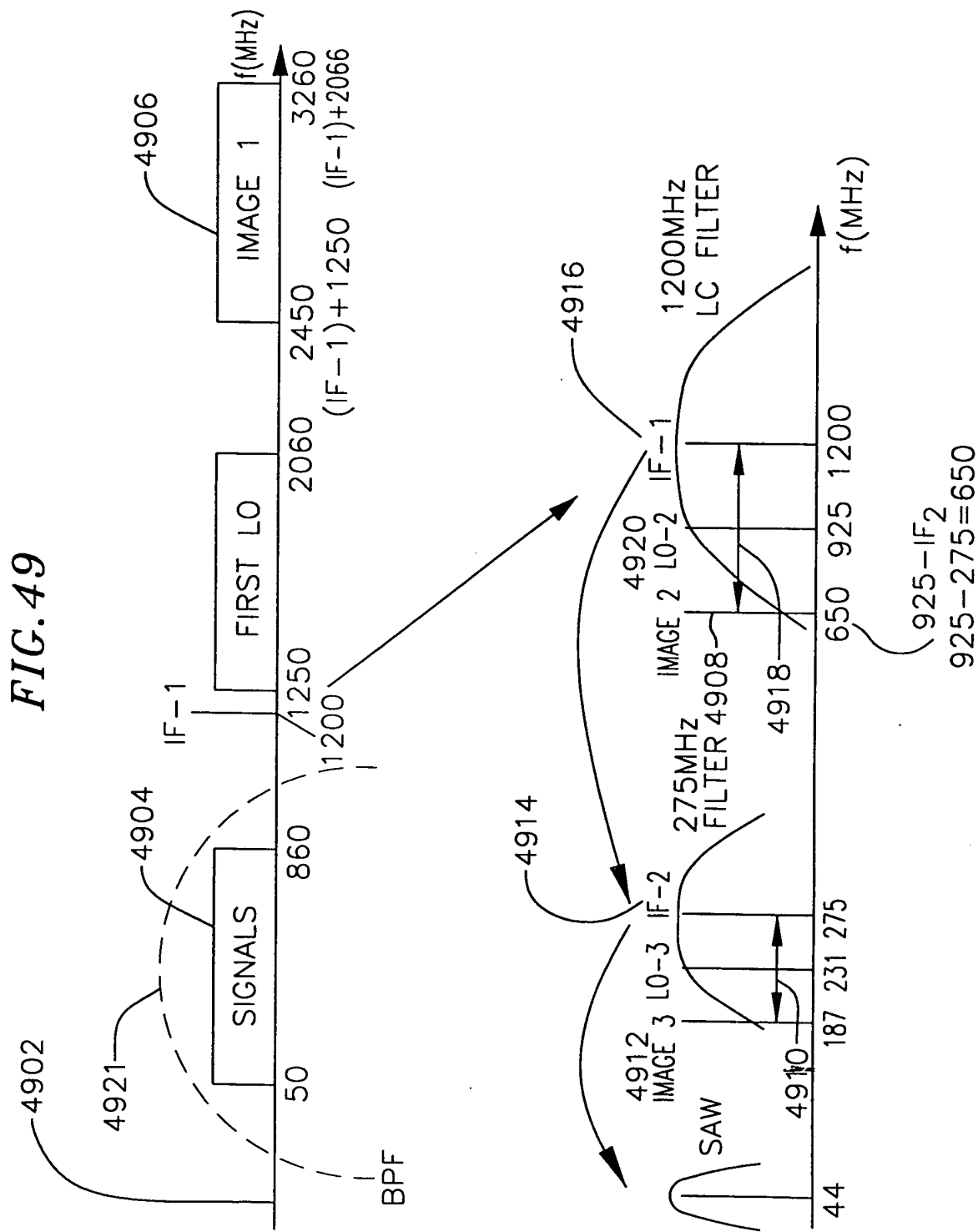


FIG. 50

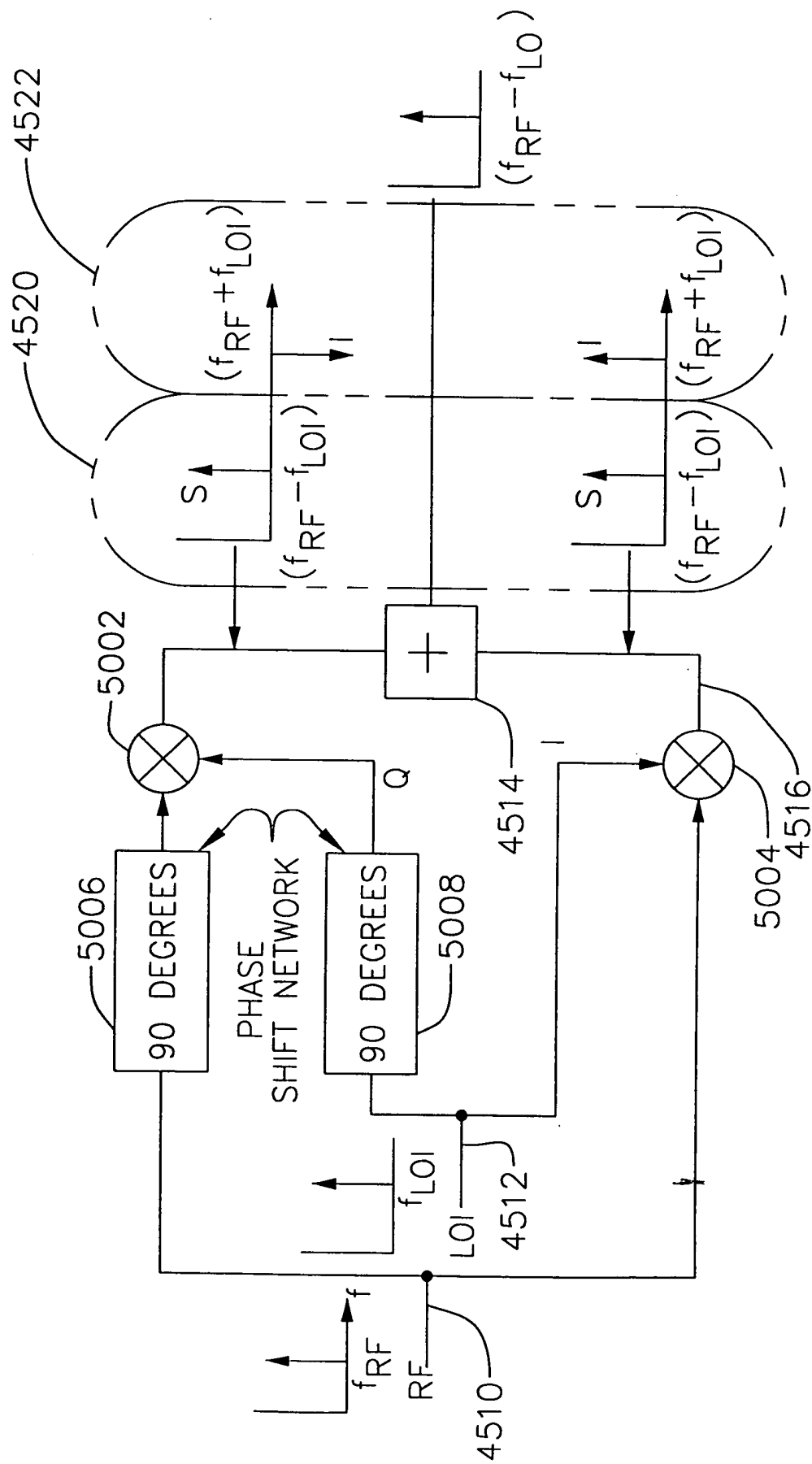


FIG. 51

EXTERNAL 36 OR 44MHz FILTER OPTION
E.C.SIEMENS X6964($f_c=43.75\text{MHz}$)

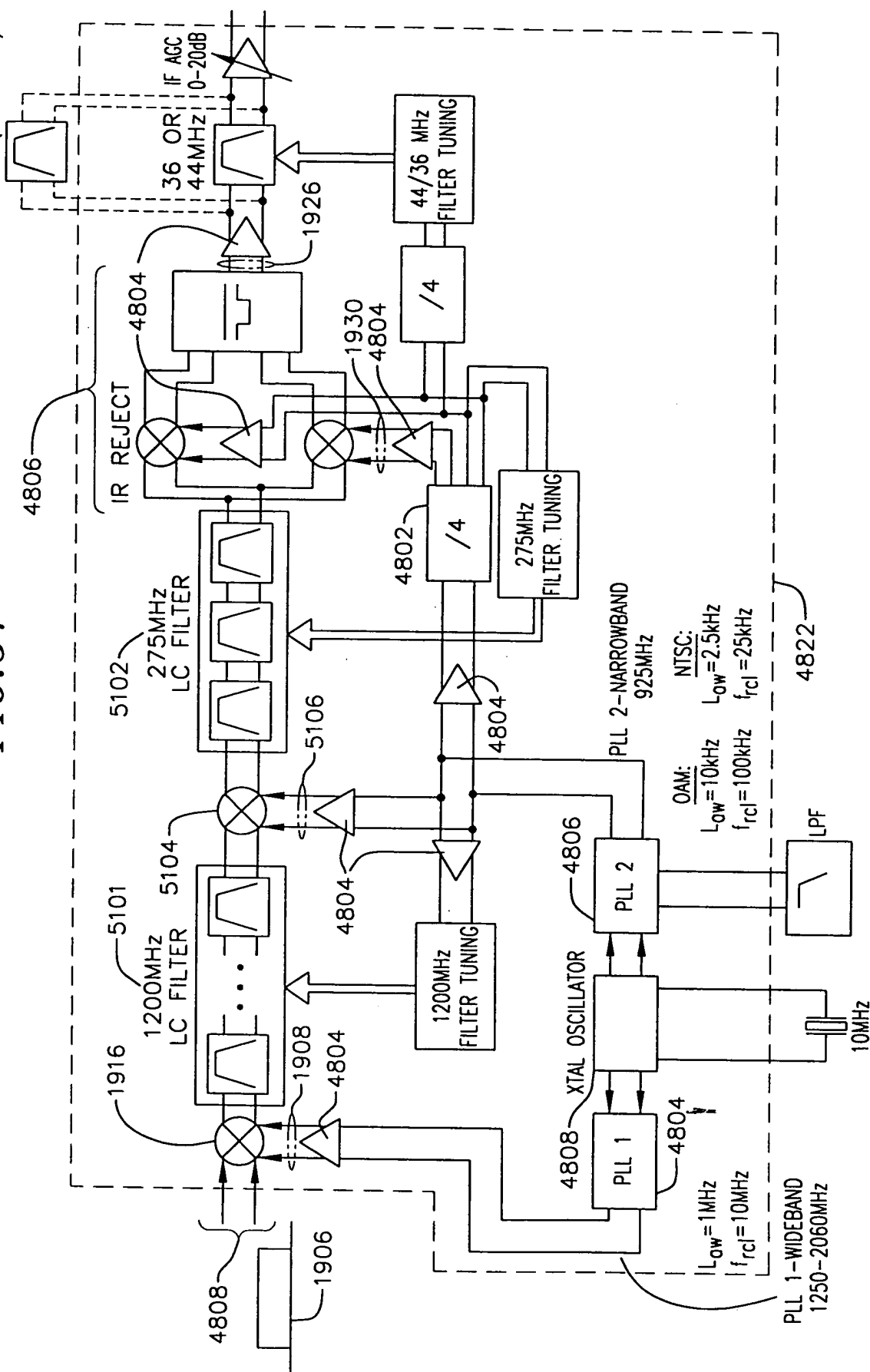


FIG. 52

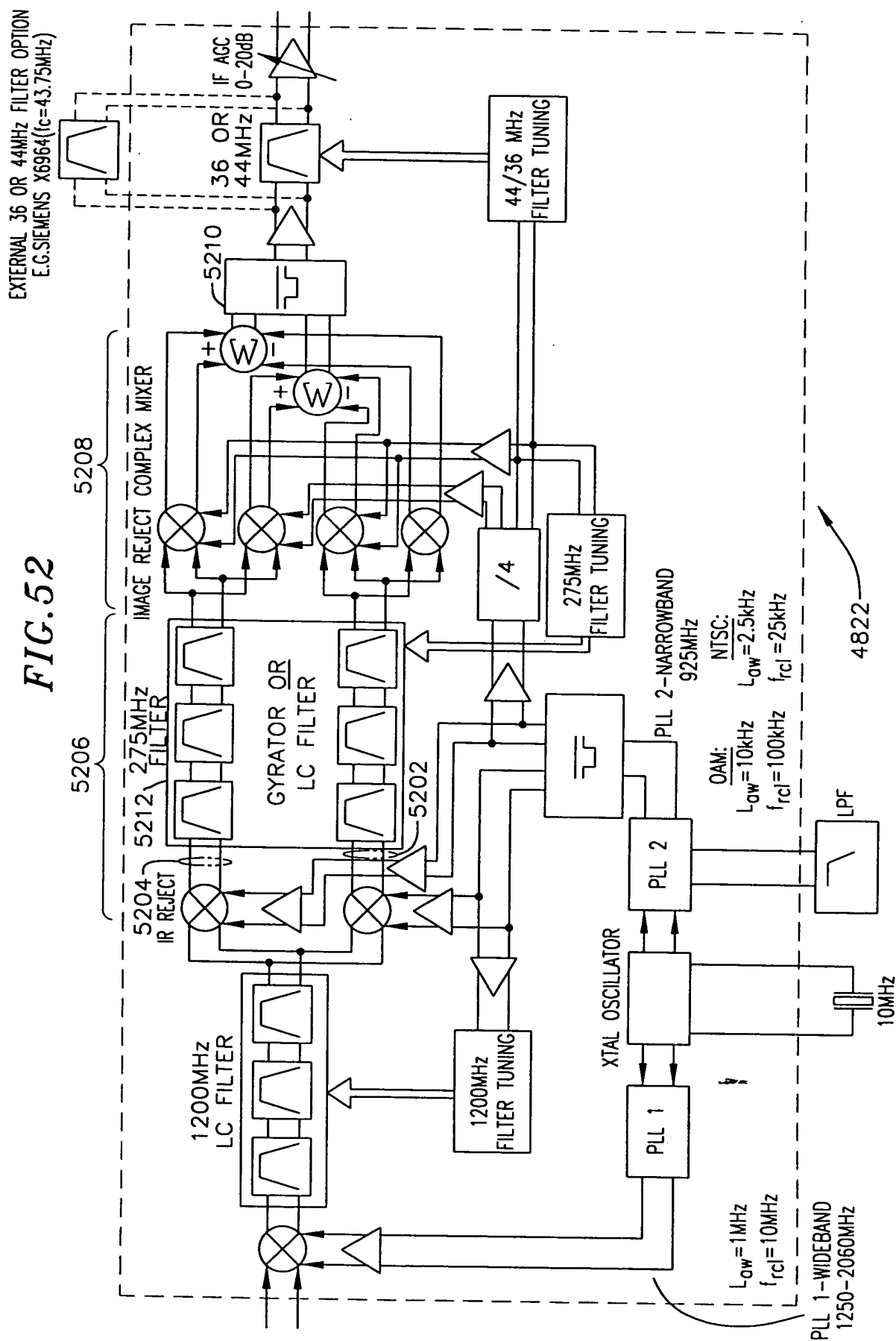


FIG.53
CATV TUNER

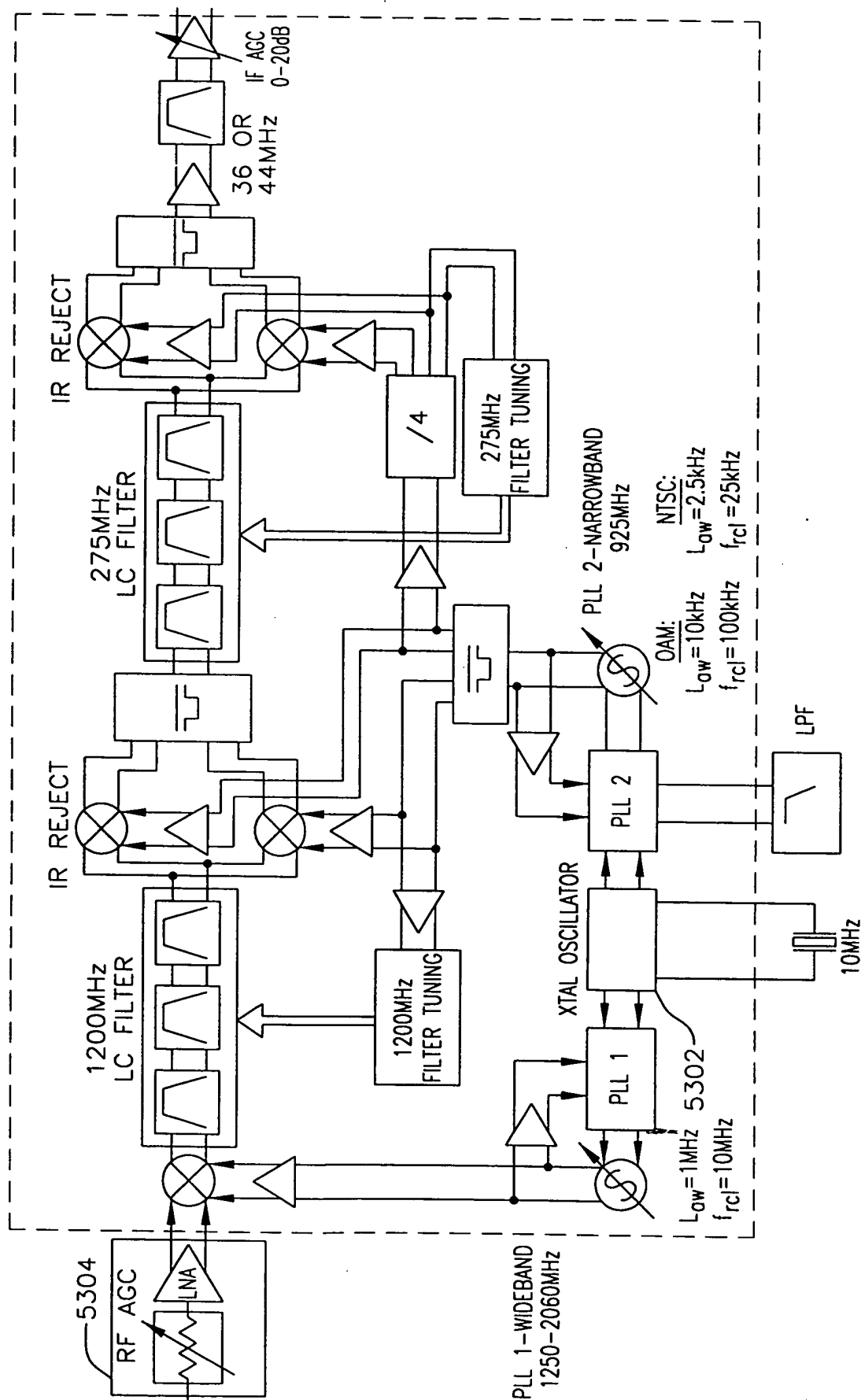
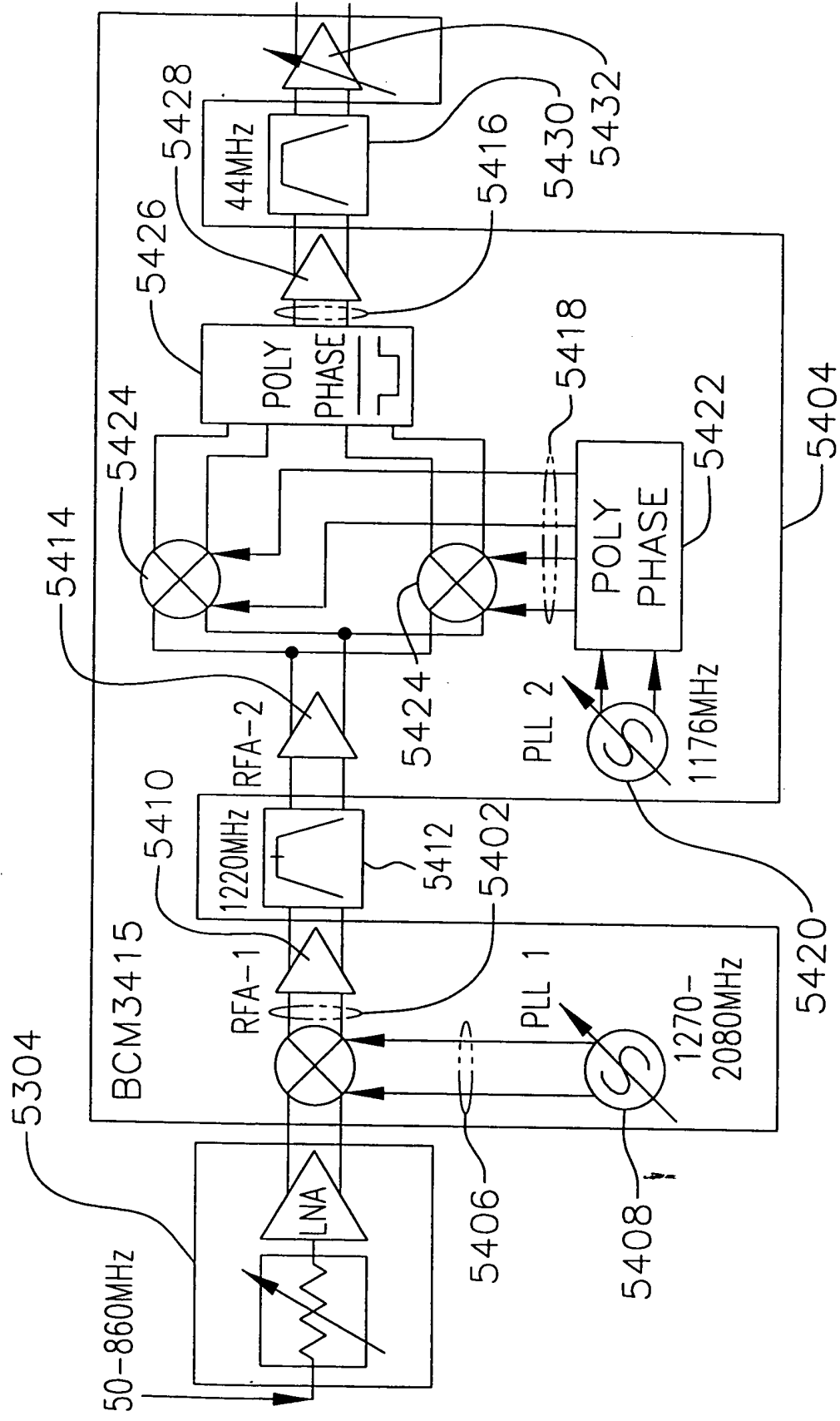


FIG. 54



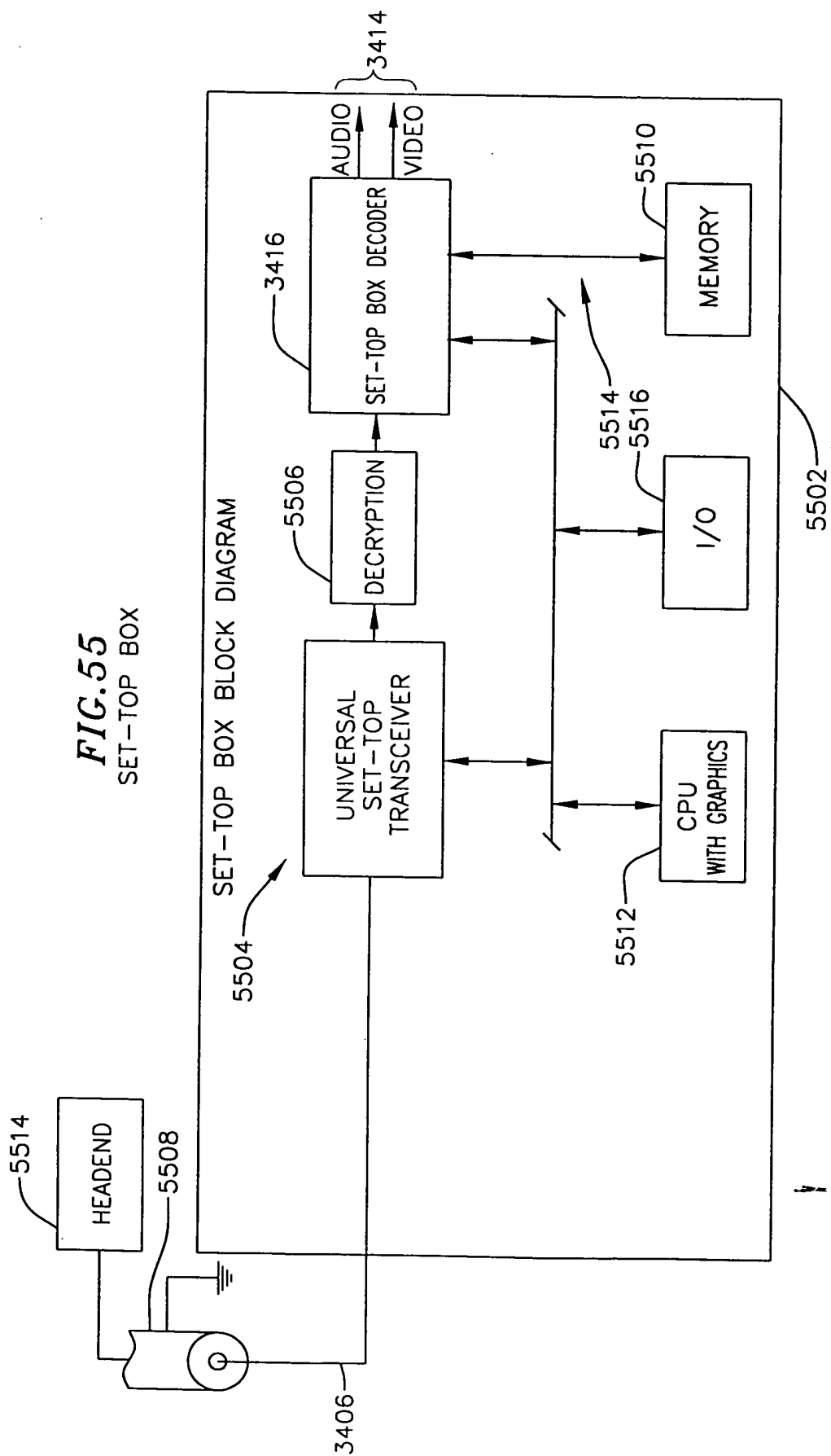


FIG. 57

VCR BLOCK DIAGRAM

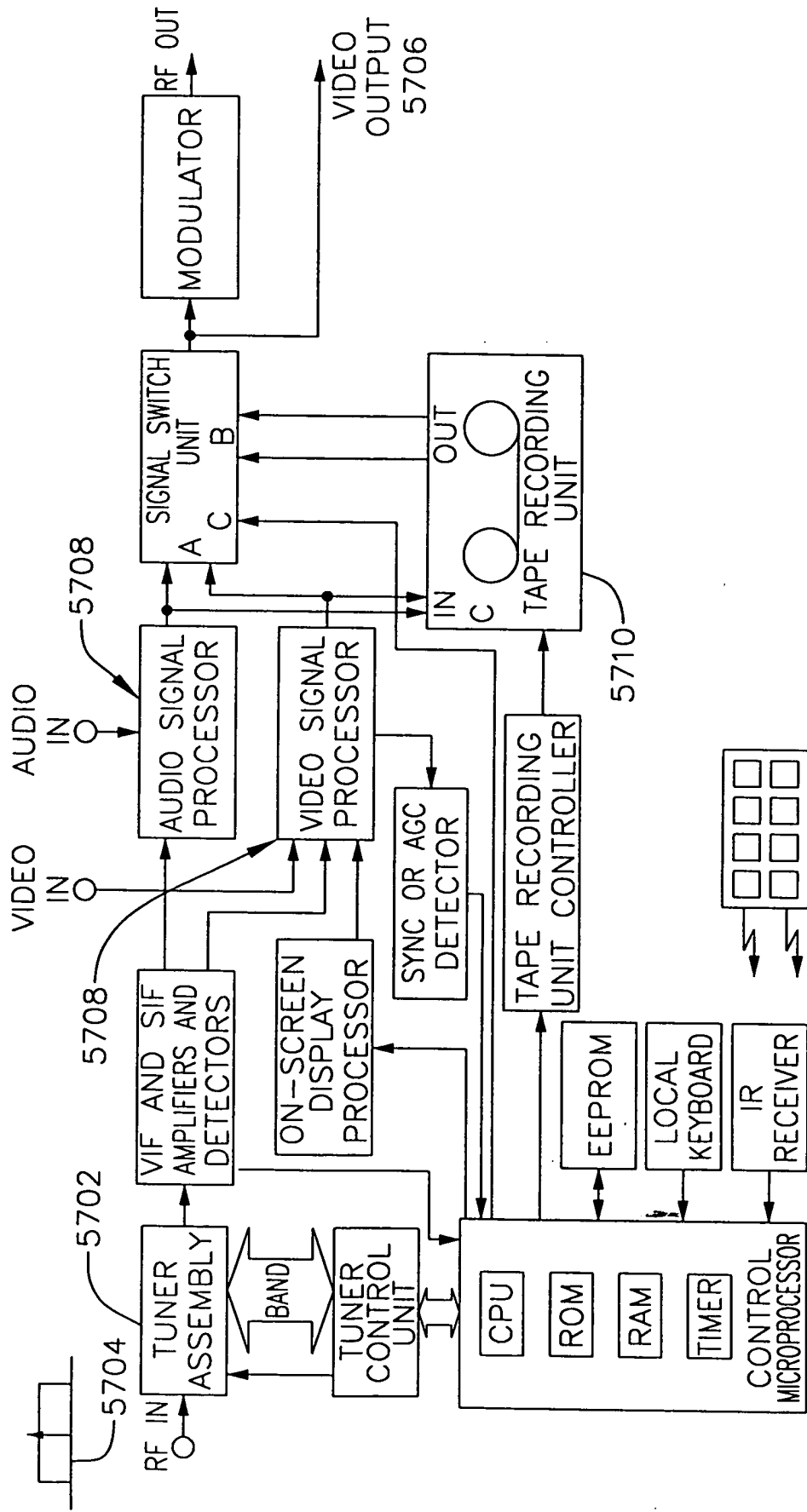


FIG. 58

